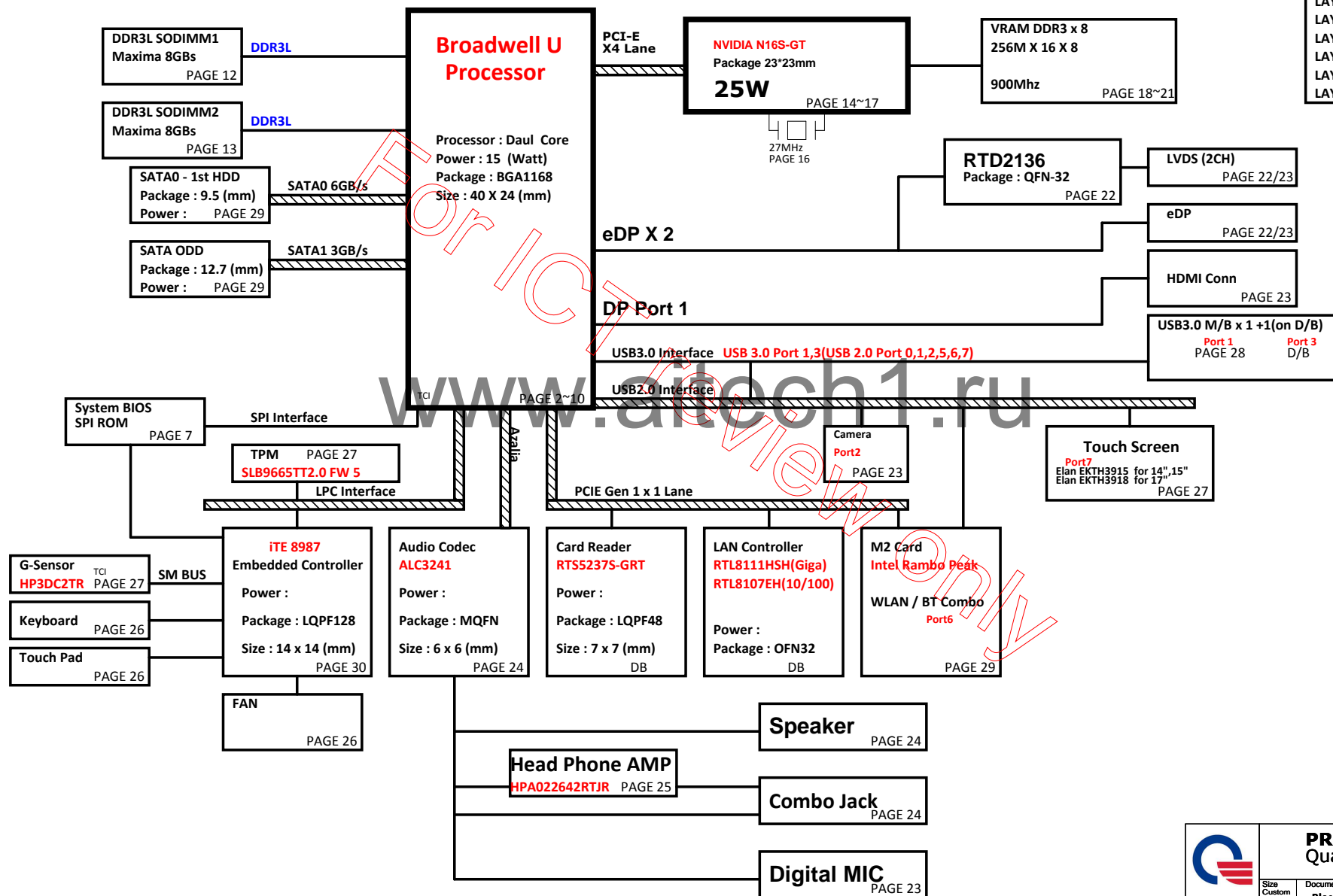


X12 DIS (14" / 15" / 17") Chocolate X12 Intel Crescent Bay ULT Platform Block Diagram

PCB 10L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : GND
LAYER 7 : IN3
LAYER 8 : IN4
LAYER 9 : GND
LAYER 10 : BOT



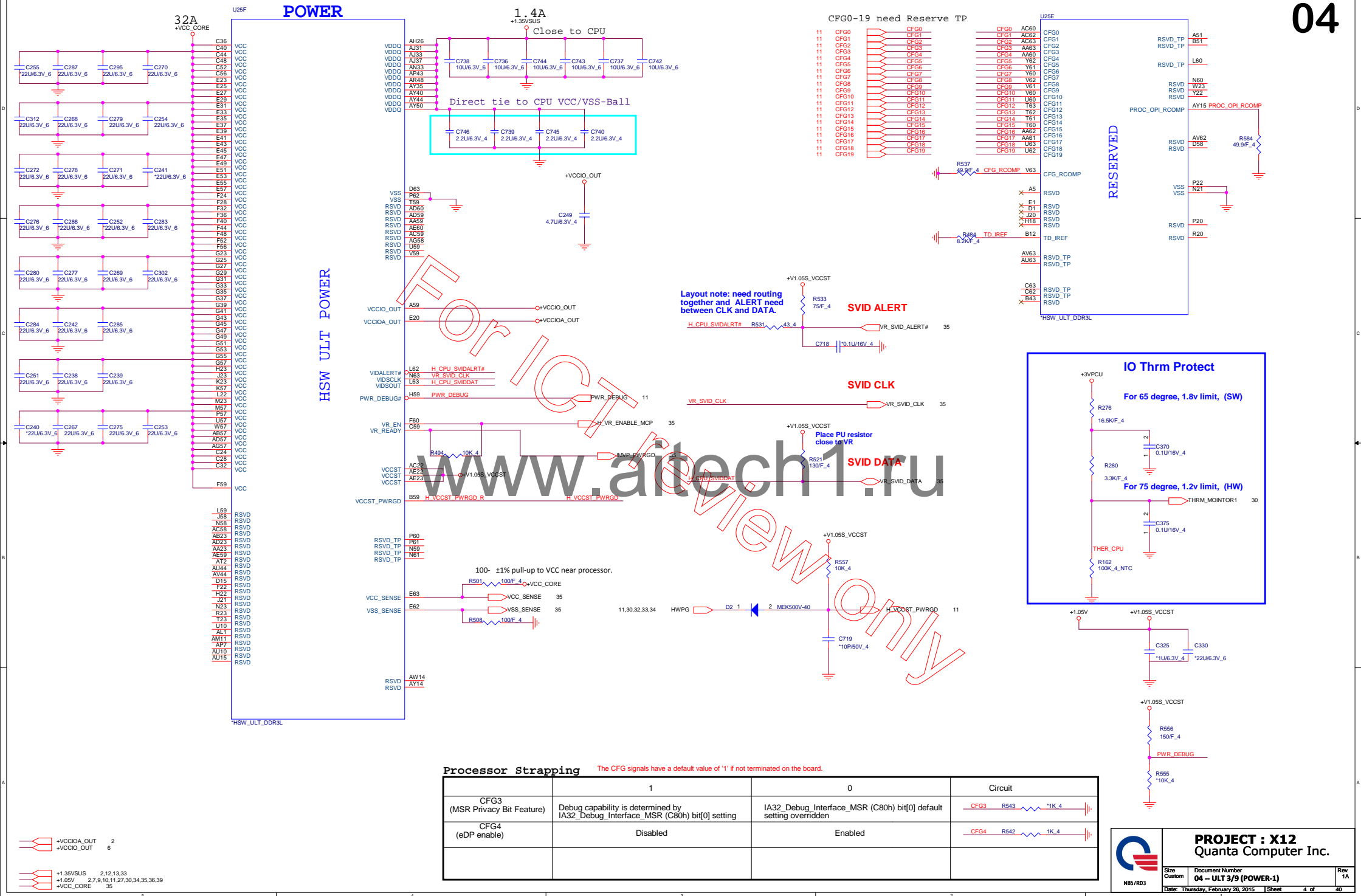
PROJECT : X12
Quanta Computer Inc.

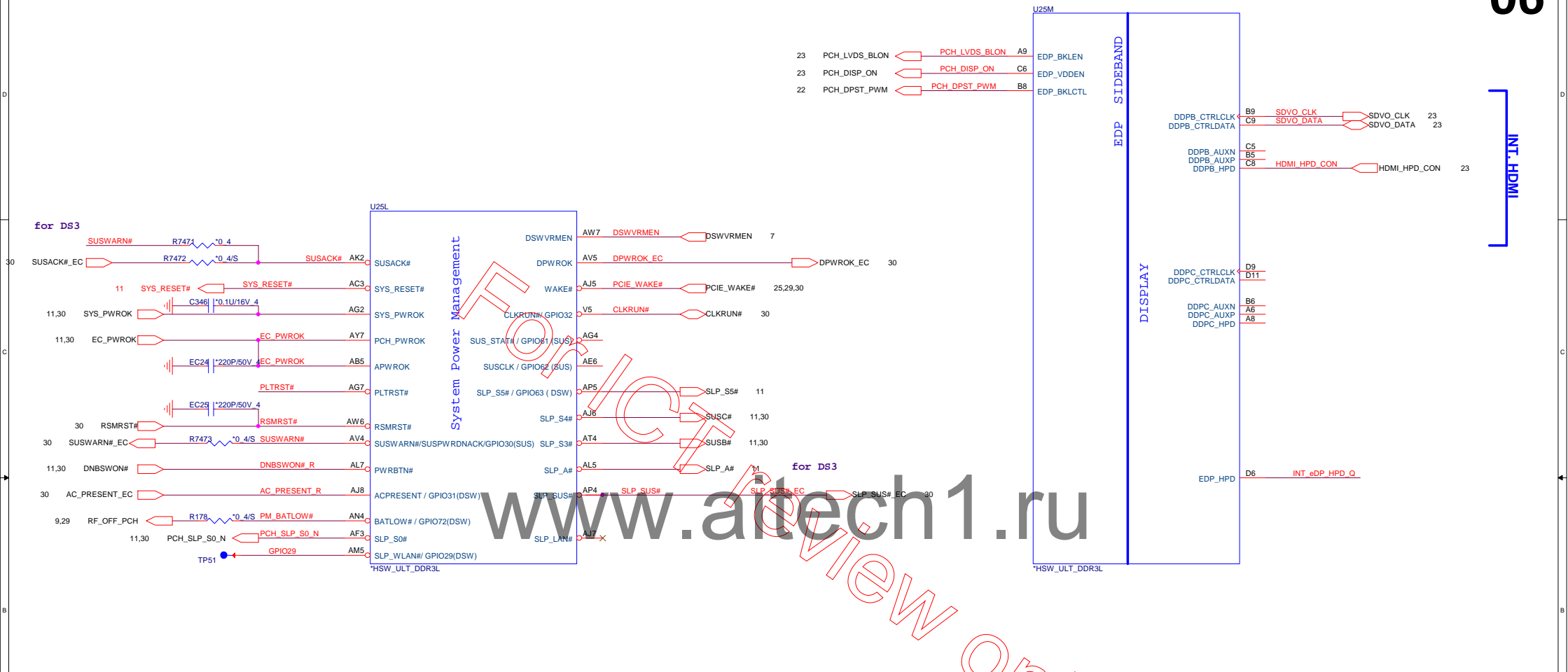
Size Custom	Document Number Block Diagram	Rev 1A
Date: Thursday, February 26, 2015	Sheet	1 of 40

NB5/RD3

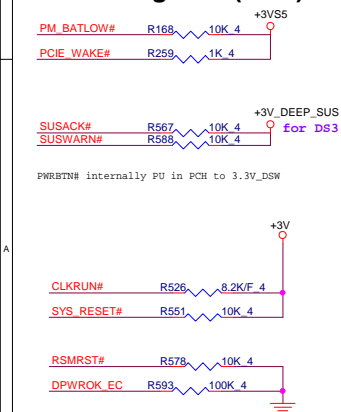
A vertical bar is divided into four segments labeled A, B, C, and D from bottom to top. An arrow points to the boundary between segments B and C.



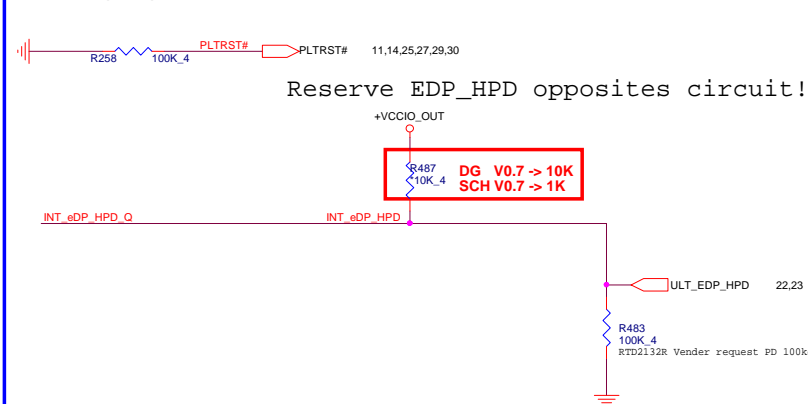




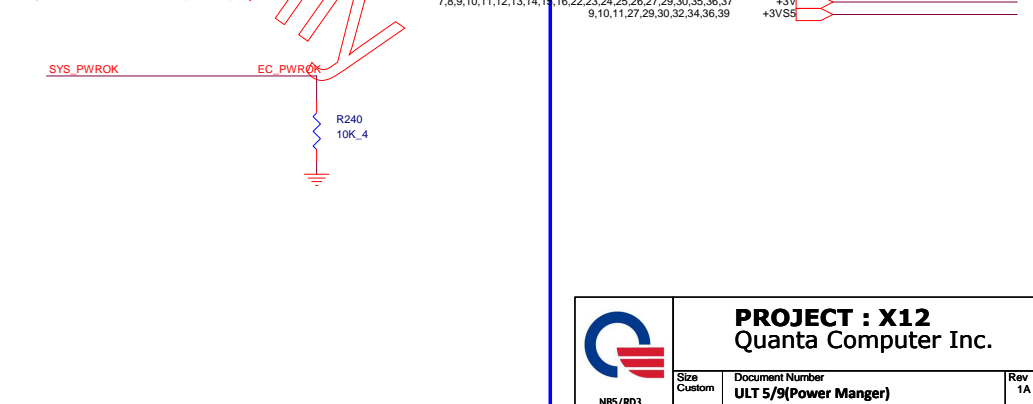
PCH Pull-high/low(CLG)



PLTRST#(CLG)



System PWR_OK(CLG)



The diagram illustrates the PCH Strap Table, showing connections between various PCH straps and system components. The components are organized into columns: RTC, LPC, AUDIO, SATA, and SPI. The connections are as follows:

- RTC:**
 - TP35: RTC_X1 (AW5), RTC_X2 (AY5), RTC_RST# (AU7), SRTC_RST# (AV6), PCH_INVRMEN (AV7)
 - 11: RTC_RST#
 - +3V_RTC: R577, 1M, 4, SM_INTRUDER# (AU6), INTRUDER# (AV7)
 - 24: ACZ_BCLK (AW8), ACZ_SYNC (AV11), ACZ_RST# (AU8)
 - ACZ_SDIN0: AY10
 - ACZ_SDOUT: AU11
 - AW10: HDA_DOCK_EN# / I2S1_TXD
 - AV10: HDA_DOCK_RST# / I2S1_SFRM
 - AY8: I2S1_SCLK
- LPC:**
 - AU12: HDA_SDIN1 / I2S1_RXD
 - AW10: HDA_DOCK_EN# / I2S1_TXD
 - AV10: HDA_DOCK_RST# / I2S1_SFRM
 - AY8: I2S1_SCLK
- AUDIO:**
 - HDA_BCLK / I2S0_SCLK (AW8)
 - HDA_SYNC / I2S0_SFRM (AV11)
 - HDA_RST# / I2S_MCLK (AU8)
 - HDA_SDIN0 / I2S0_RXD (AY10)
 - HDA_SDIN1 / I2S1_RXD (AU12)
 - HDA_SDO / I2S0_TXD (AU11)
 - HDA_DOCK_EN# / I2S1_TXD (AW10)
 - HDA_DOCK_RST# / I2S1_SFRM (AV10)
 - I2S1_SCLK (AY8)
- SATA:**
 - SATA_RXN0 (J5), SATA_RXP0 (H5), SATA_TXN0 (B15), SATA_TXP0 (A15)
 - SATA_RXN2 (J8), SATA_RXP2 (H8), SATA_TXN2 (A17), SATA_TXP2 (B17)
 - SATA_RXN0 (J5), SATA_RXP0 (H5), SATA_TXN0 (B15), SATA_TXP0 (A15)
 - SATA_RXN2 (J8), SATA_RXP2 (H8), SATA_TXN2 (A17), SATA_TXP2 (B17)
 - SATA_RXN0 (J5), SATA_RXP0 (H5), SATA_TXN0 (B15), SATA_TXP0 (A15)
 - SATA_RXN2 (J8), SATA_RXP2 (H8), SATA_TXN2 (A17), SATA_TXP2 (B17)
 - SATA_RXN0 (J5), SATA_RXP0 (H5), SATA_TXN0 (B15), SATA_TXP0 (A15)
 - SATA_RXN2 (J8), SATA_RXP2 (H5), SATA_TXN0 (B15), SATA_TXP0 (A15)
- SPI:**
 - PCH_SPI1_CLKA3: SPI_CLK
 - PCH_SPI1_CS0# Y7: SPI_CS0#
 - PCH_SPI1_CS1# X4: SPI_CS1#
 - PCH_SPI1_CS2# X4: SPI_CS2#
 - PCH_SPI1_SI A2: SPI_MOSI
 - PCH_SPI1_SO A4: SPI_MISO
 - PCH_SPI1_IO2 Y6: SPI_IO2
 - PCH_SPI1_IO3 AF1: SPI_IO3

The diagram also includes a large red watermark "www.4everpcb.com" and a "TCL" logo.

Pin Name	Strap description	Sampled	Configuration	Circuit						
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode							
SDIO_D0 /GPIO66	Top-Block Swap	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)							
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up							
HDA_SDO /I2S0_TXD	Flash Descriptor Security Only for Interposer	PWROK	0 = Default (weak pull-down 20K) 1 = Can be Overriden							
GSPI0_MOSI /GPIO86	Boot BIOS Selection	PWROK	<table border="1"> <thead> <tr> <th>GNT0#</th><th>Boot Location</th></tr> </thead> <tbody> <tr> <td>1</td><td>LPC</td></tr> <tr> <td>0</td><td>SPI(Default)</td></tr> </tbody> </table>	GNT0#	Boot Location	1	LPC	0	SPI(Default)	
GNT0#	Boot Location									
1	LPC									
0	SPI(Default)									
GPIO15	TLS Confidentiality	PWROK	0 = ME Crypto Transport Layer Security cipher suite with no confidentiality(Default) 1 = Intel ME Crypto TLS cipher suite with confidentiality							
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	ALWAYS	Should be always pull-up							

no stuff If use green Clock

[illegible]

+3V_DEEP_SUS R574 *1K 4 ACZ_SYNC
 24 ACZ_SYNC_AUDIO R585 33 4 ACZ_SYNC
 24 ACZ_RST#_AUDIO R590 33 4 ACZ_RST#
 24 ACZ_SDOUT_AUDIO R589 33 4 ACZ_SDOUT
 24 BIT_CLK_AUDIO R591 33 4 ACZ_BCLK
 C741
 *10P50V_4

ACC_LED# R538 10K 4
 SIO_EXT_SM# R528 10K 4
 PCI_SERR# R527 10K 4
 SATA3GP R550 10K 4

Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

TP21 ● PCH SPI CS0# R

TP22 ● PCH SPI1 CLK R

TP23 ● PCH SPI1 SI R

TP24 ● PCH SPI1 SO R

TP25 ● BIOS WP#

TP25 ● HOLD#

TP25 ●

PCH SPI CS0# R488 15/F 4 PCH SPI CS0# R 1

PCH SPI1 CLK R488 15/F 4 PCH SPI1 CLK R 6

PCH SPI1 SI R488 15/F 4 PCH SPI1 SI R 5

PCH SPI1 SO R488 15/F 4 PCH SPI1 SO R 2

R457/R453/R450/R451/R546/R548 close to U15 pin

C716 22P/50V_4

C714 0.1U/16V_4

C713 1U/6.3V 4 +3VSPI R491 3.3K/F 4

PCH SPI IO2 R430 15/F 4 BIOS WP#

+3V DEEP_SUS

U24

CE# VDD 8 +3VSPI

SCK HOLD# 7 HOLD#

SI SO

WP# VSS 4

GD25B64BSIGR

AKES3EFPON07

R500 3.3K/F 4

R504 15/F 4

PCH SPI IO3

+3V

+5V

+1.05V 2,4,9,10,11,27,30,34,35,36

+3VS5 6,9,10,11,27,30,32,34,36

+3VPCU 4,25,26,27,29,30,31,32

+3V_RTC 10,27

+V1_0SS_ASATA3PLL 10

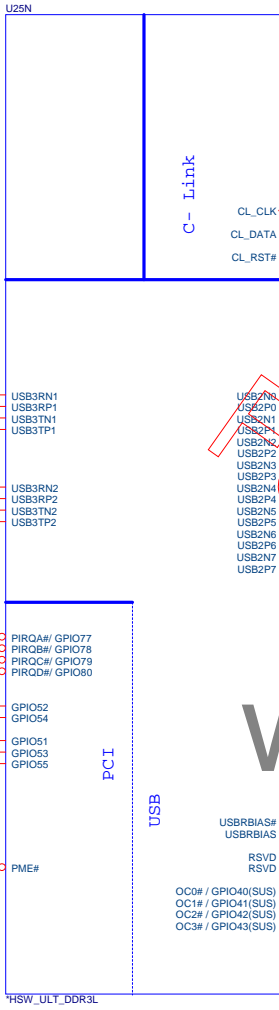
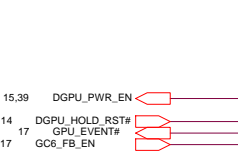
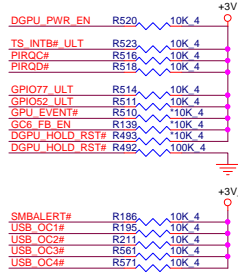
PROJECT : X12

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Lynx Point-LP Platform Controller Hub
(HDA, JTAG, SATA)

PCI/USBOC# Pull-up(CLG)



Cardreader

WLAN

LAN

USB2.0(M/B-1) (USBP1)

USB2.0 Small board (USBP5)

USB2.0 Small board (USBP5)

Camera

WLAN

LAN

VGA

USB

Cardreader

WLAN

LAN

VGA

USB

Cardreader

WLAN

LAN

VGA

USB

Cardreader

WLAN

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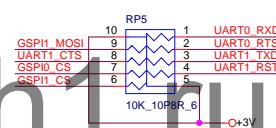
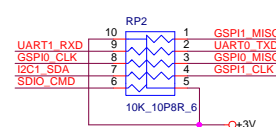
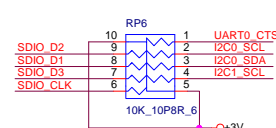
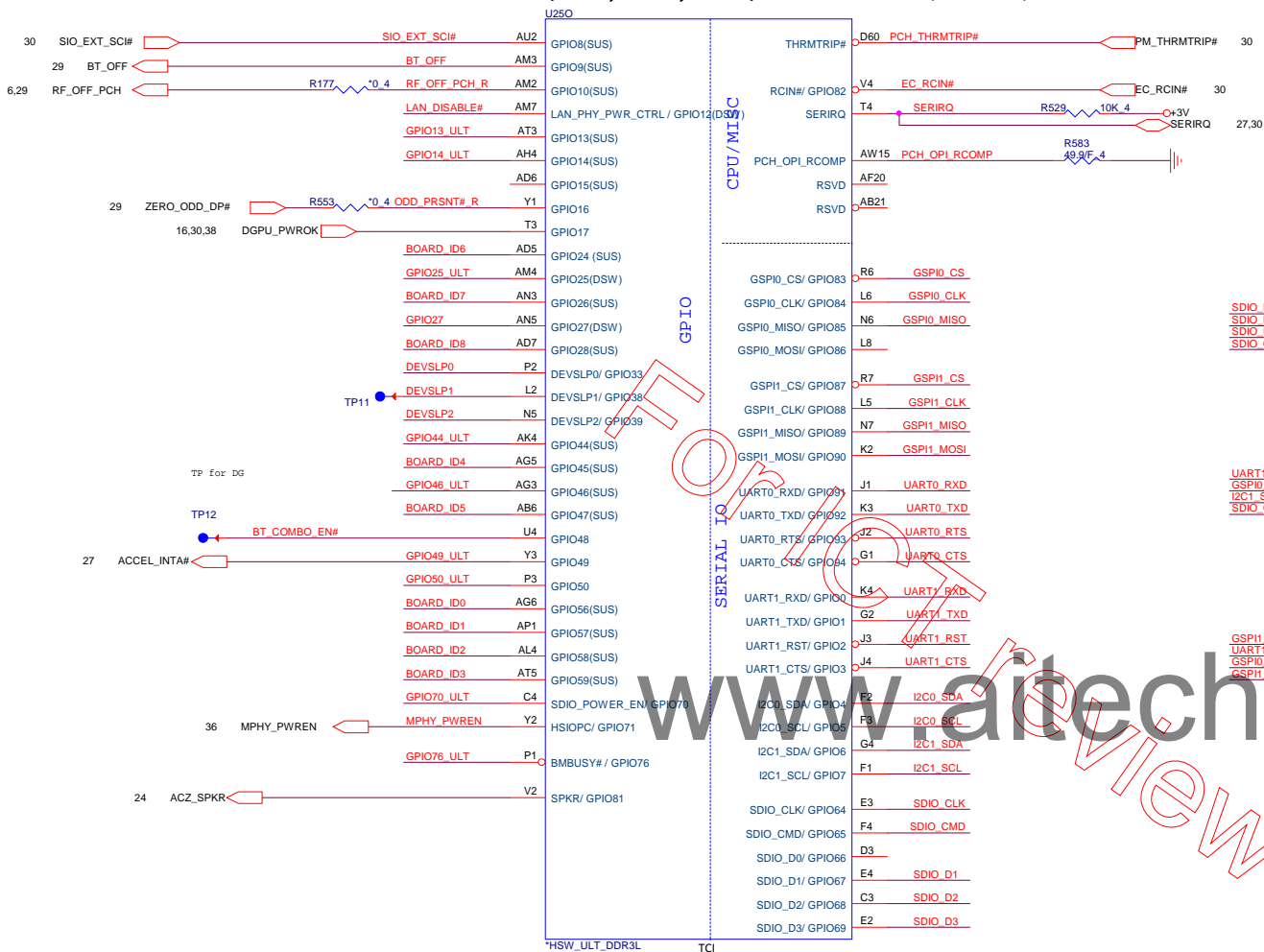
WLAN

LAN

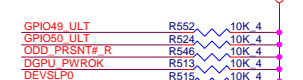
VGA

USB

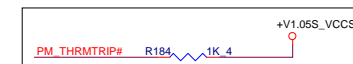
Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA) Haswell (GPIO)



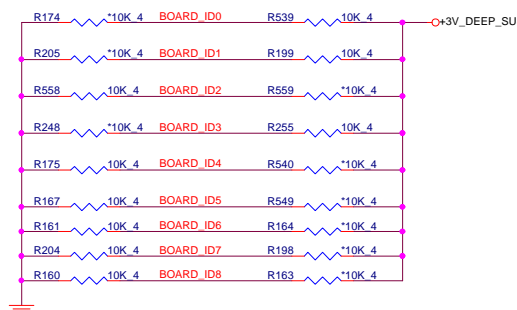
GPIO Pull-up/Pull-down(CLG)



Close to EC



Model	BOARD_ID[8:7]	BOARD_ID[6:5]	Board ID [4:3]	BOARD_ID[2:1]	BOARD_ID0
Definition	Reserve (Default = 00)	Reserve (Default = 00)	00 Single Rank (X12) 01 Dual Rank (X12) 10 Meso-AMD (X11) 11 Reserve	00 14" 01 15" 10 17"	0 : UMA 1 : DIS



6,7,8,10,11,12,13,14,15,16,22,23,24,25,26,27,29,30,35,36,37
6,10,11,27,29,30,32,34,36,39

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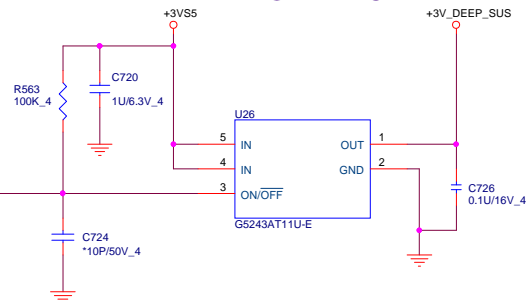
Size Custom

Document Number
ULT 8/9 (GPIO/MISC)

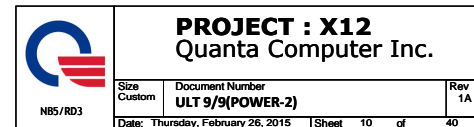
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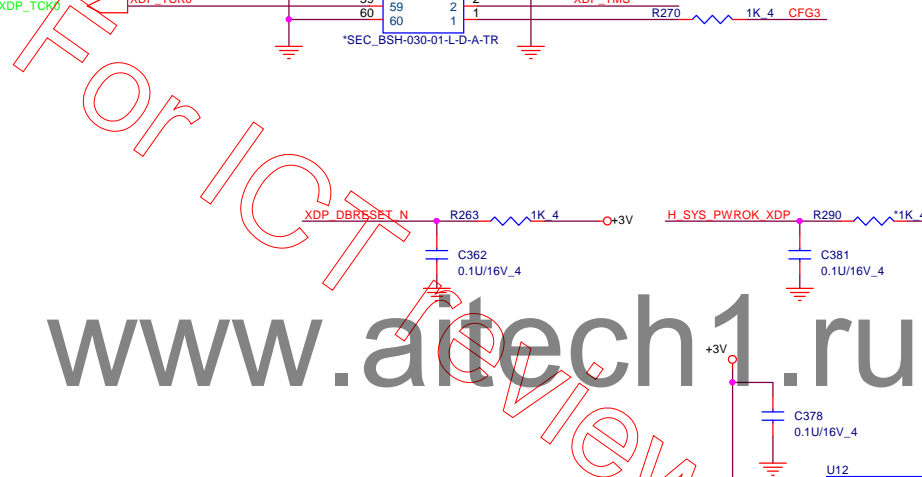
Rev 1A

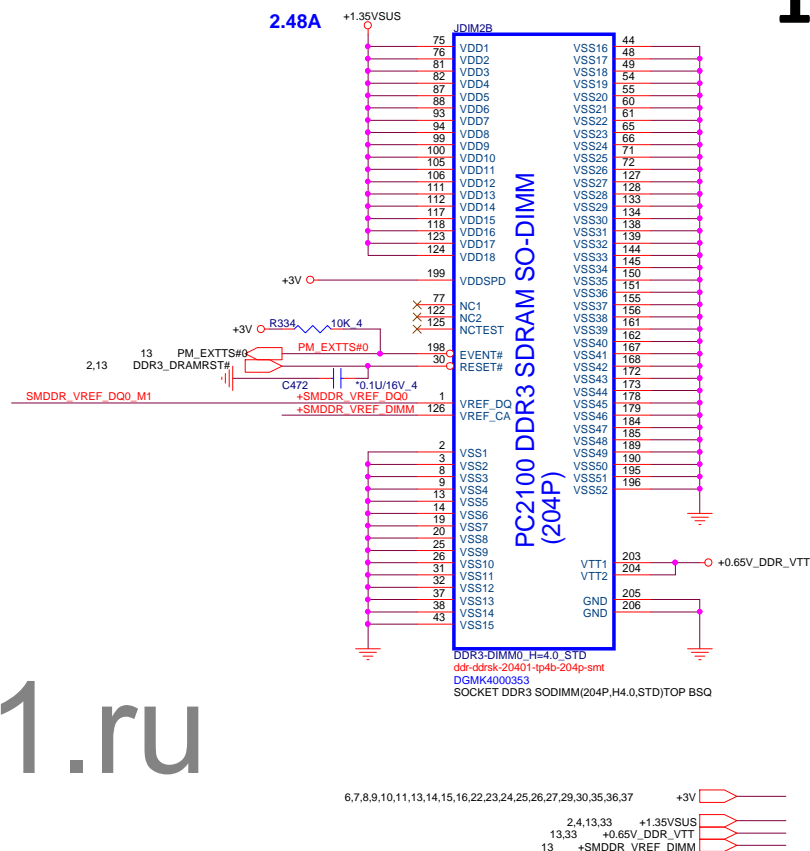
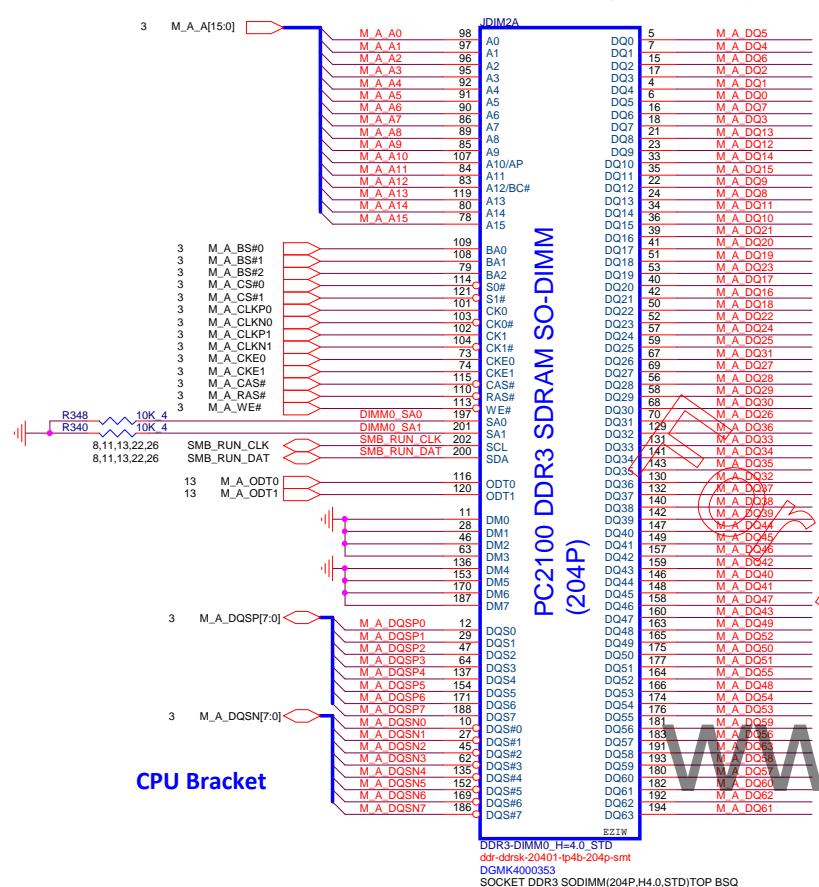
Sheet 9 of 40



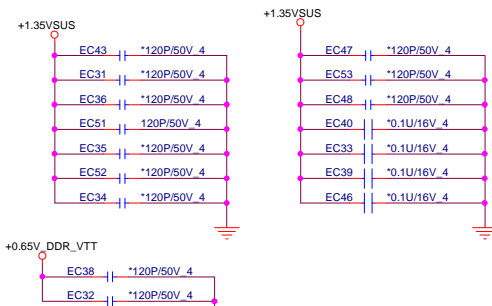
6,7,8,9,11,12,13,14,15,16,22,23,24,25,26,27,29,30,35,36,37	+3V	
23,24,25,26,27,29,36	+5V	8 +V1.05S_AUSB3PLL 7 +V1.05S_ASATA3PLL 8 +V1.05S_AXCK_LCPPLL
2,4,7,9,11,27,30,34,35,36,39	+1.05V	7.27 +3V_RTC
6,9,11,27,29,30,32,34,36,39	+3V5S	2,4,12,13,33 +1.35VSUS
13,25,27,28,32,33,34,35,36,37,38,39	+5V5S	





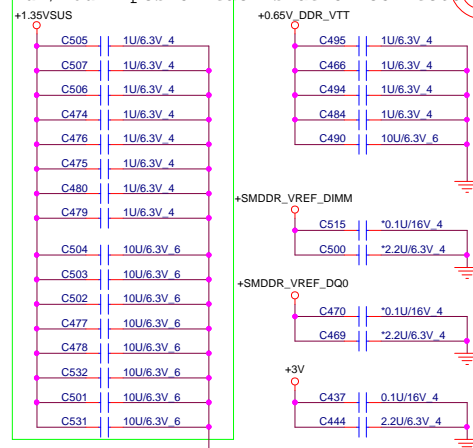


For EMI RESERVE

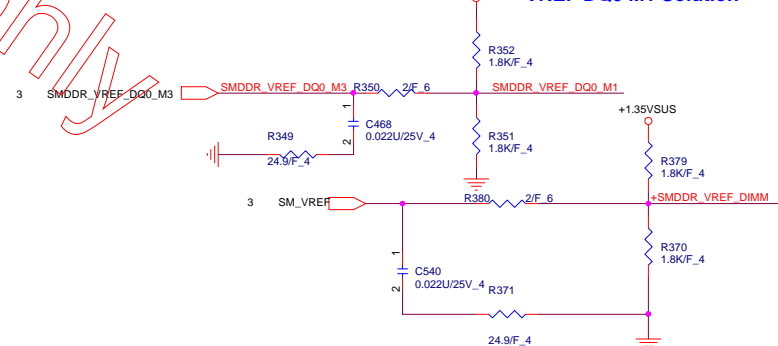


Place these Caps near So-Dimm0.

1uF/10uF 4pcs on each side of connector

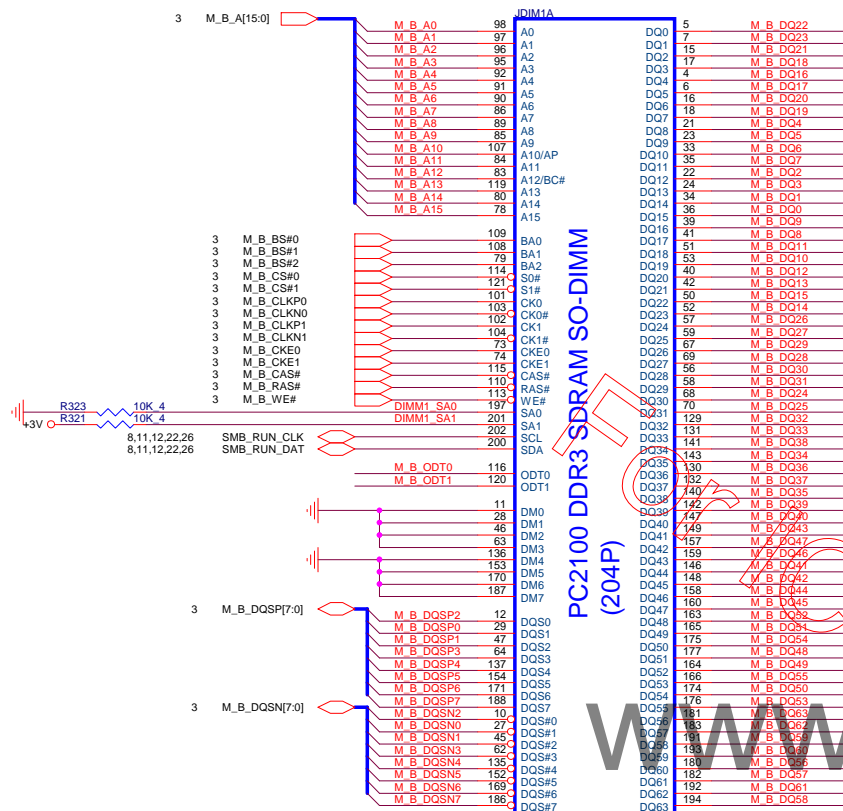


VREF DQ0 M1 Solution



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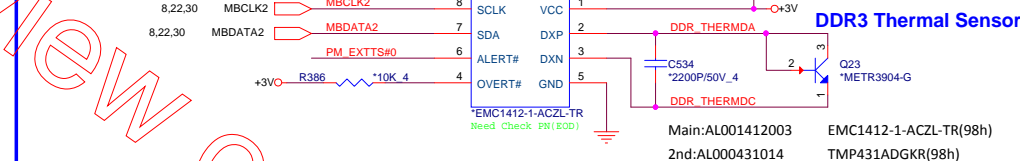
Size Custom	Document Number DDR3 DIMM0-STD(4.0H)	Rev 1.
Date: Thursday, February 26, 2015	Sheet 12 of 40	



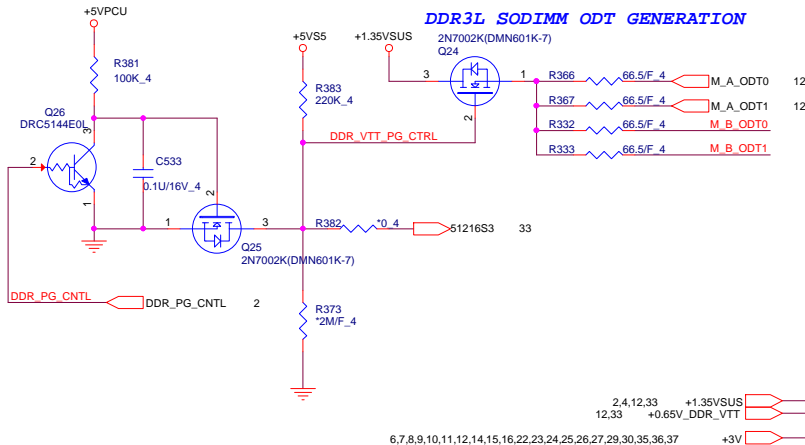
DDR3-DIMM1_H=4.0_RVS
ddr-ddr3k-20401-tp4b-204p-smt
DGMK4000264

Local Thermal Sensor

MY可移除

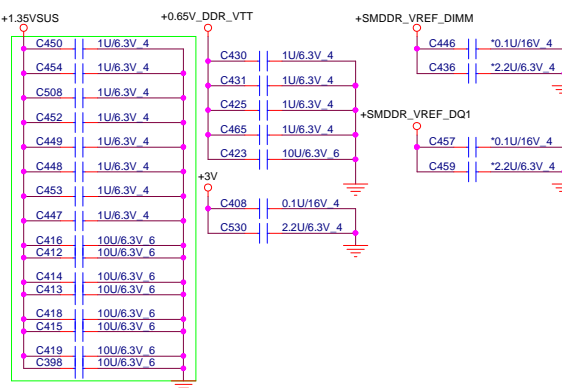


DDR3L SODIMM ODT GENERATION

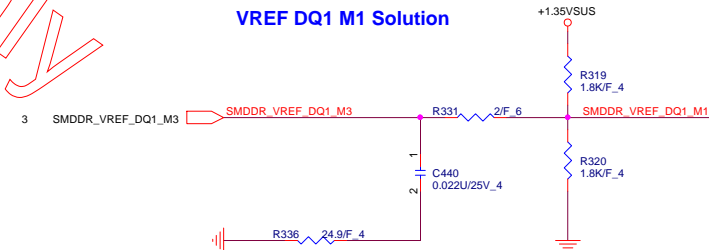


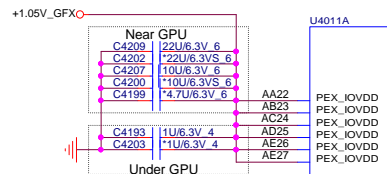
Place these Caps near So-Dimm1.

1uF/10uF 4pcs on each side of connector

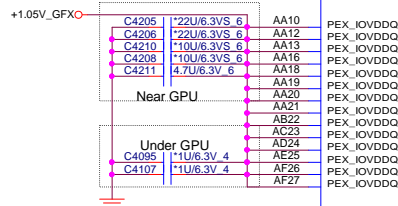


VREF DQ1 M1 Solution

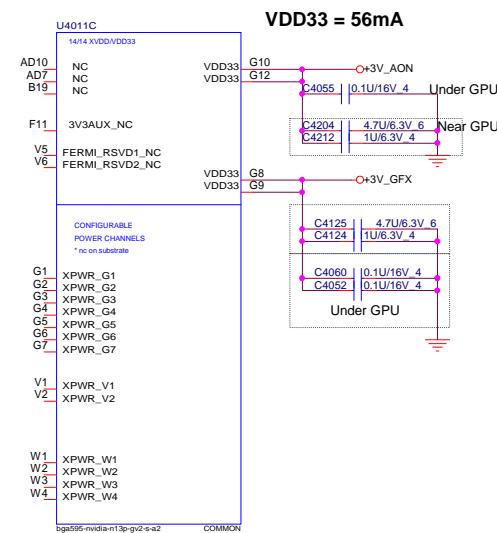
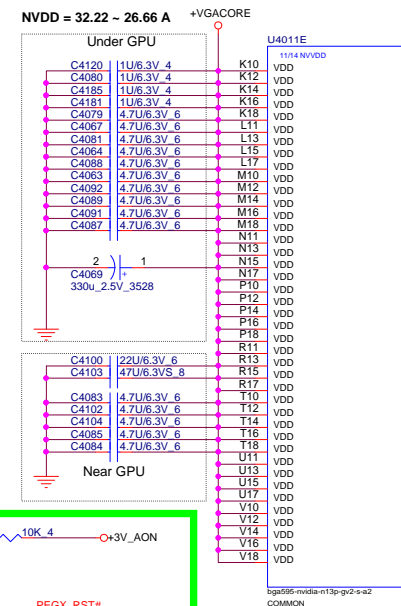
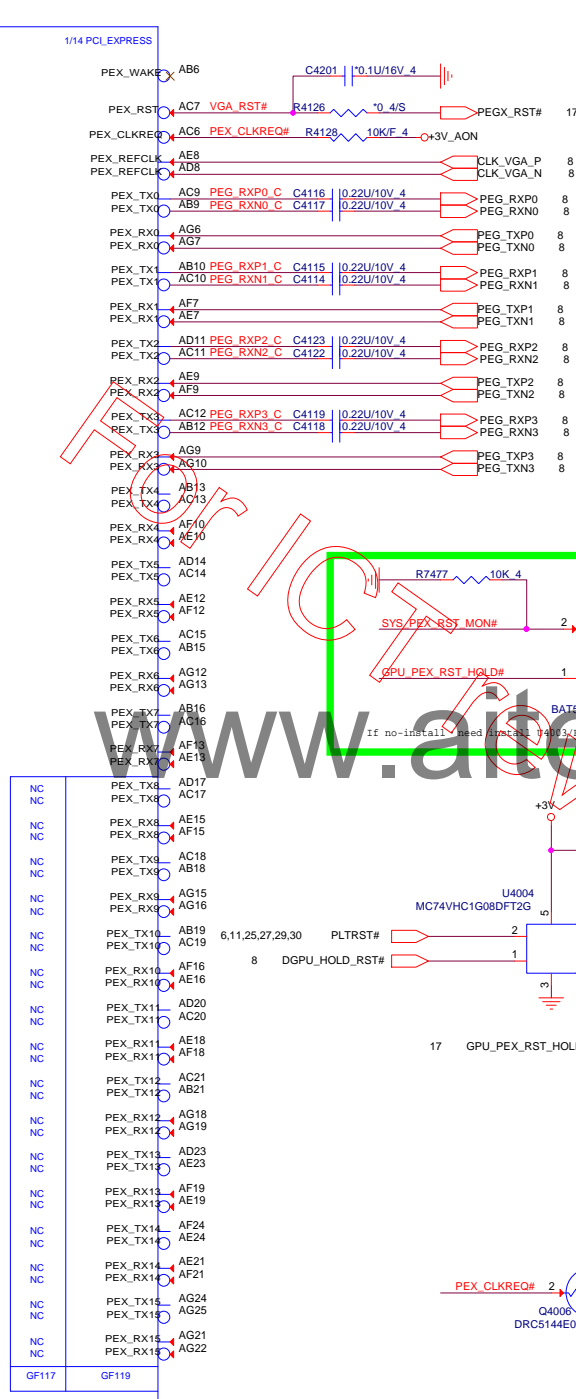
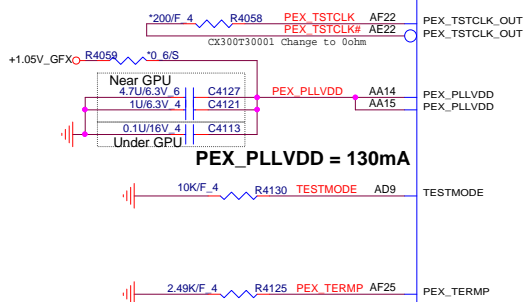
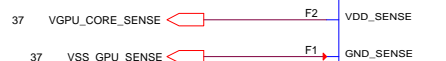
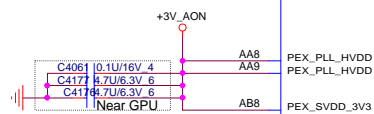




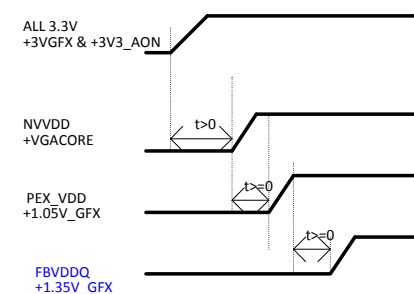
PEX_IOVDD + PEX_IOVDDQ = 1.042A



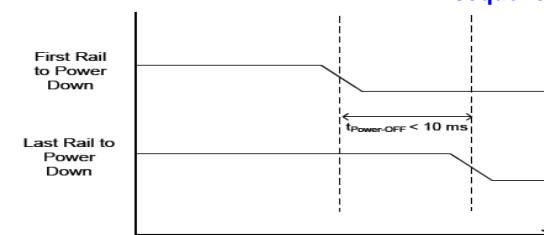
PEX_PLL_HVDD +
PEX_SVDD_3V3 = 143mA



Power up sequence

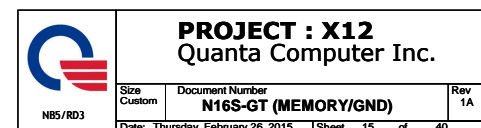


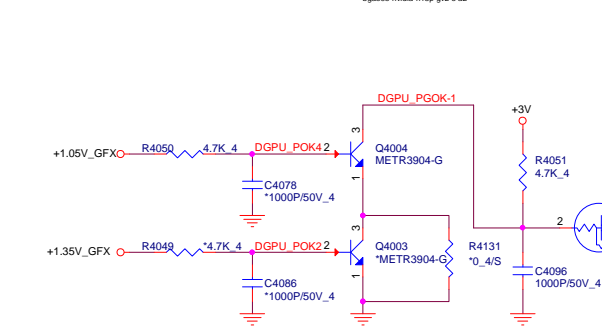
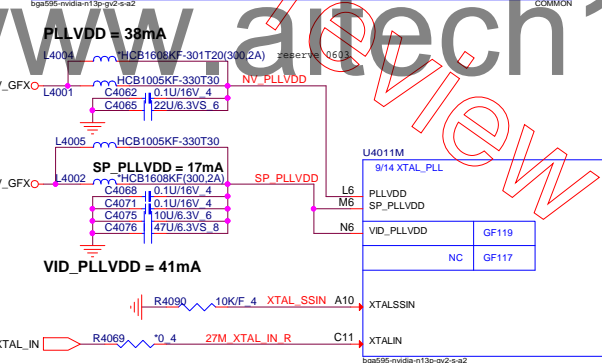
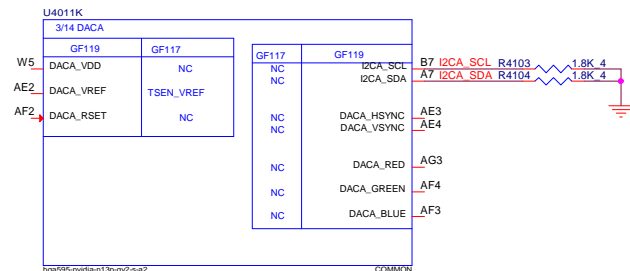
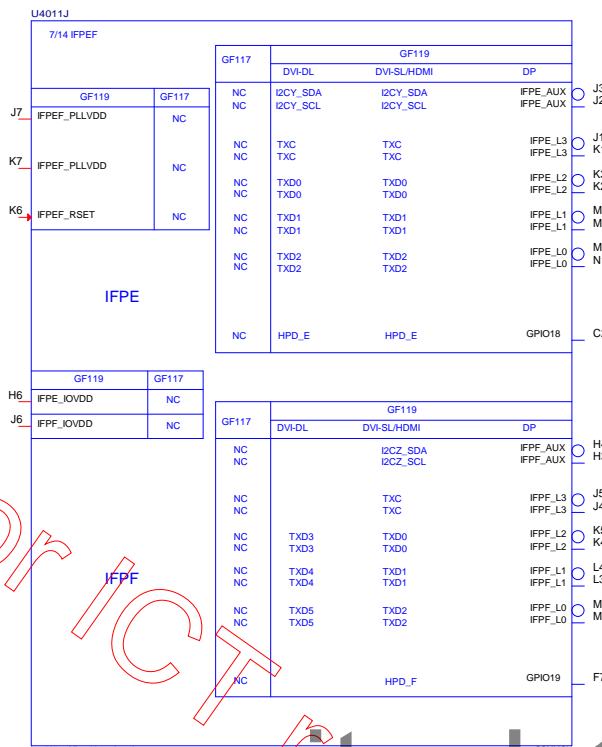
Power down sequence

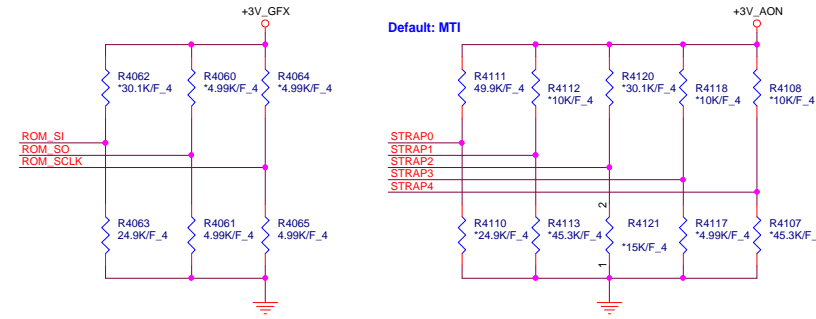


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Size Custom	Document Number N16S-GT (PCIE I/F) /NVDD	Rev 1A
Date: Thursday, February 26, 2015		Sheet 14 of 40





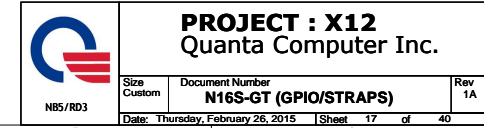


Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

RAM Configuration Table		ROM	SI	E				
RAMCFG (3:0)	DESCRIPTION	Vendor	Vendor P/N	256Mx16 Strap	128Mx16 Strap	QBC	TOP B/S	
1110	DDR3L 256Mx16, 64bit, 4Gb,900MHz	HYNIX	MT42C4G63CFR-N0C	0XE	TBD	AKD5PZDTW01	AKD5PZDTW01	
0011	DDR3L 256Mx16, 64bit, 4Gb,900MHz	Micron	MT41J1256M16HA-093G:E	0x4	TBD	AKD5PZSTU02	AKD5PZSTU00	
1111	DDR3L 256Mx16, 64bit, 4Gb,900MHz	SAMSUNG	K4W4G1646E-BC1A	0xF	TBD	AKD5PGDT501	AKD5PGDT500	

GPIO ASSIGNMENTS

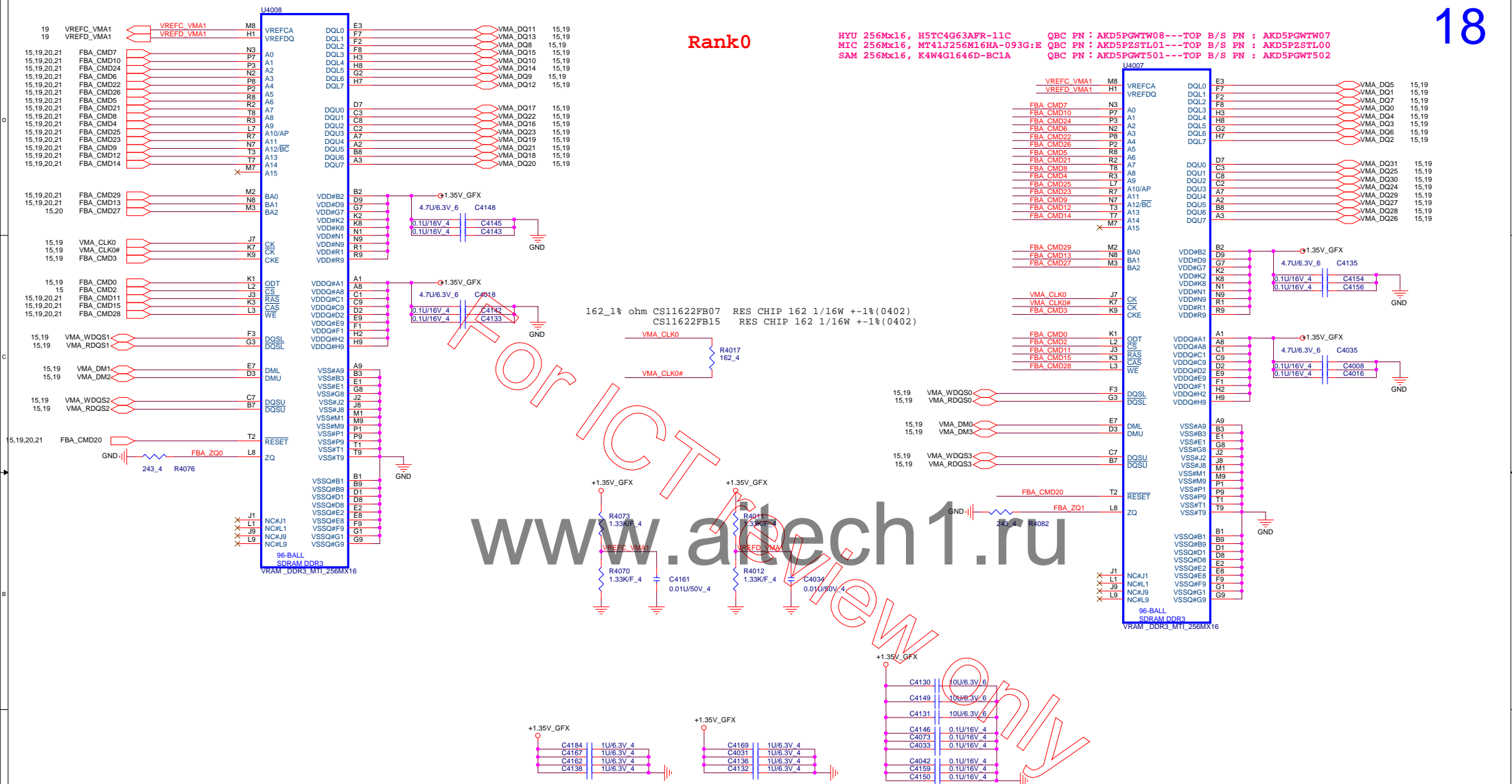
GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D_VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMORY_VREF CONTROL
11	OUT	PWR_VID	GPU_CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding



Rank0

HYU 256Mx16, H5TC4G63APR-11C
 MIC 256Mx16, MT41J256M16BA-093G:E
 SAM 256Mx16, K4W4G1646D-BC1A

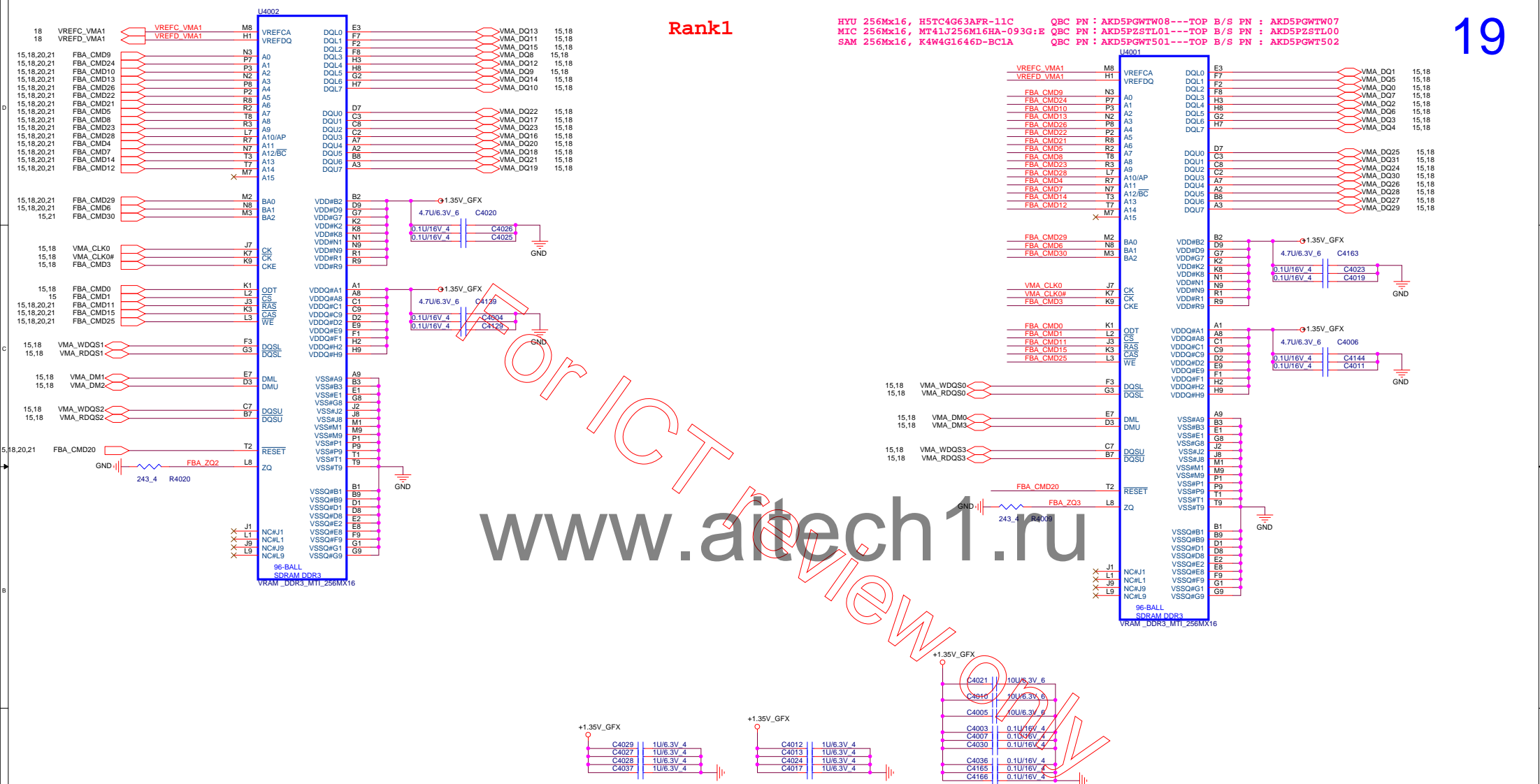
QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
 QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
 QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502



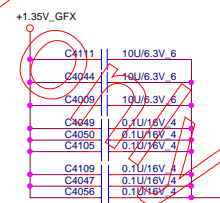
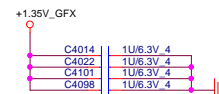
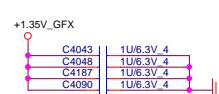
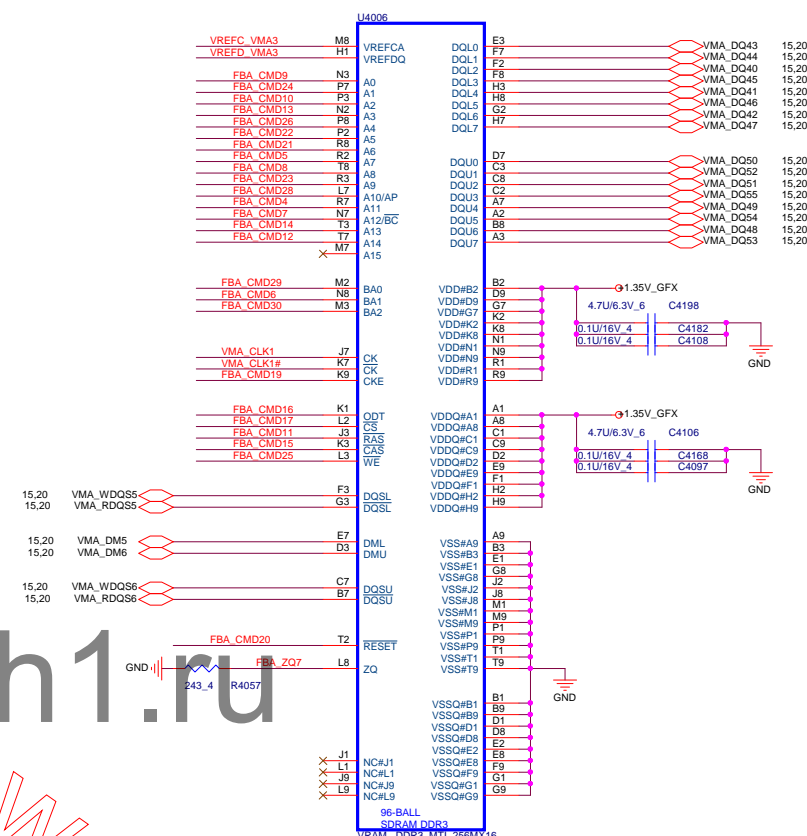
PROJECT : X12
Quanta Computer Inc.

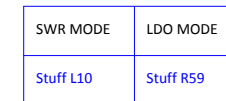
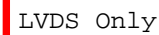
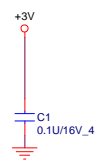
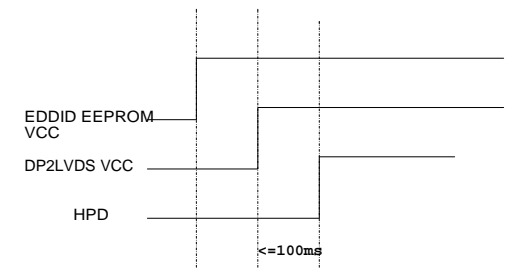
Size Custom Document Number DDR3L - RANK0 Rev 1A
 Date: Thursday, February 26, 2015 Sheet 18 of 40

Rank1

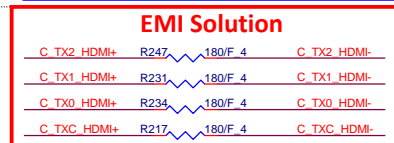
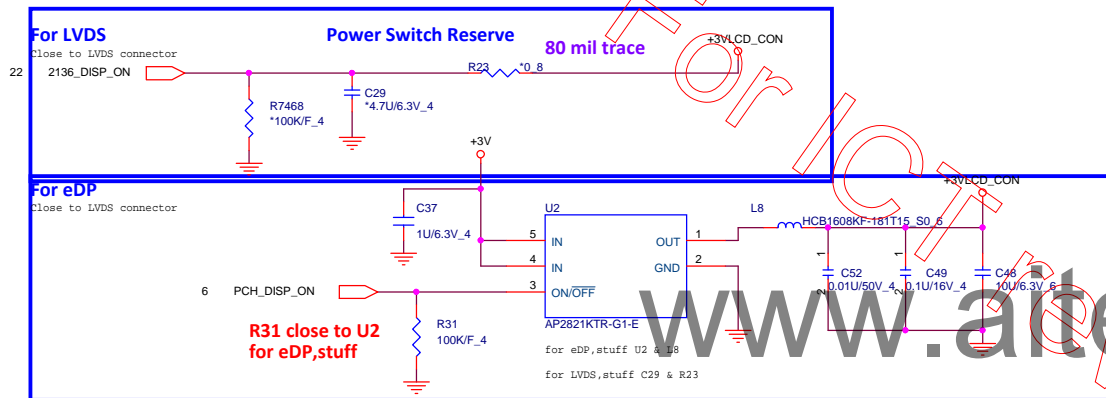
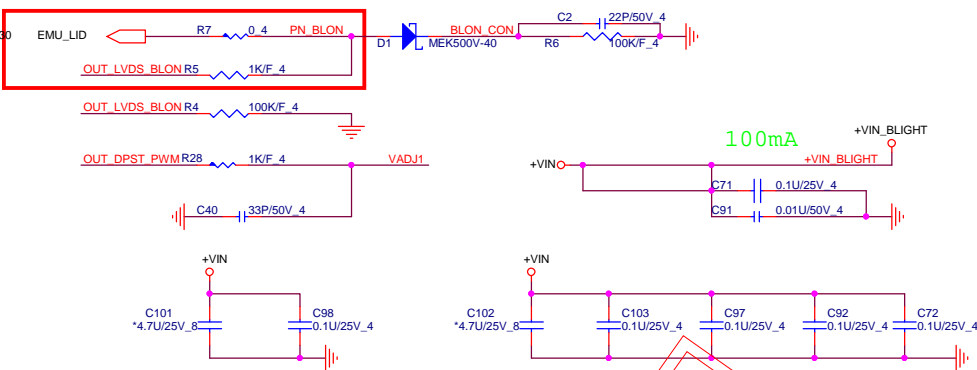


HYU 256Mx16, H5TC4G63AFR-11C QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
SAM 256Mx16, K4W4G1646D-BC1A QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502

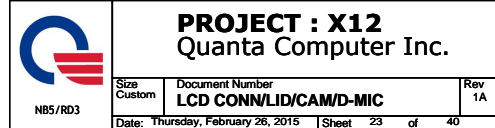
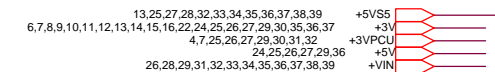
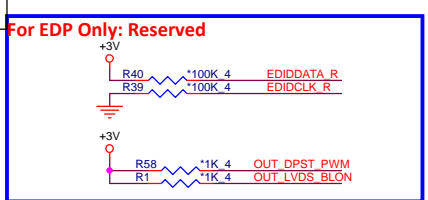
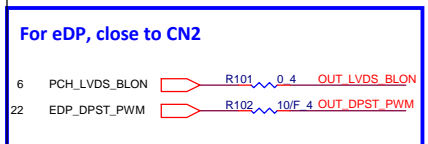
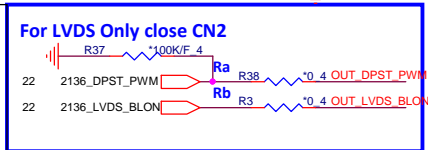
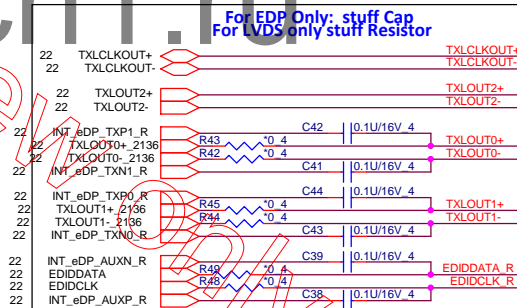
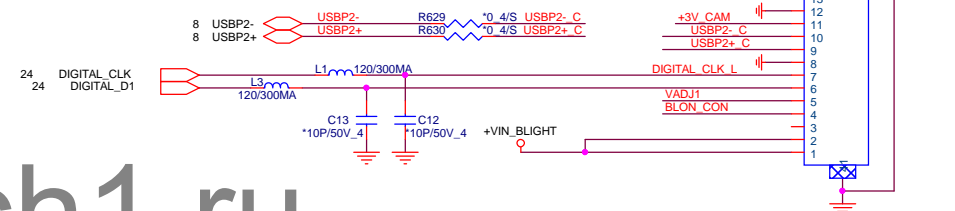
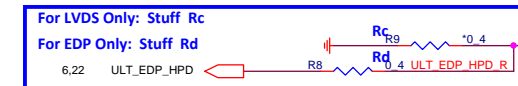
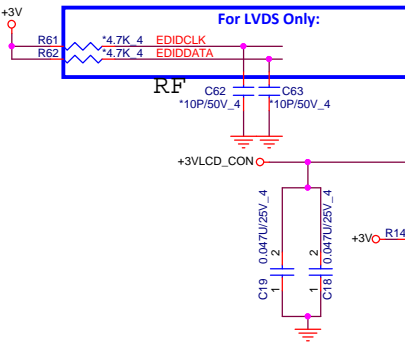
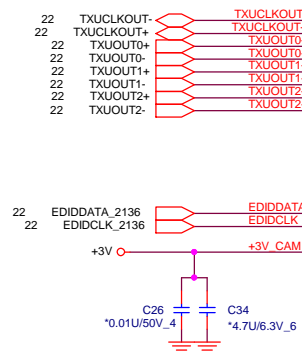
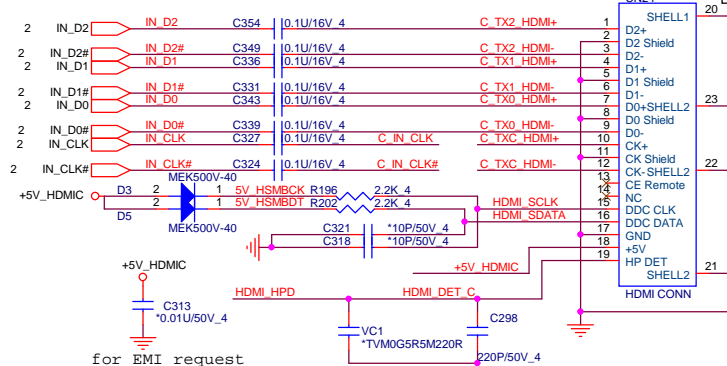
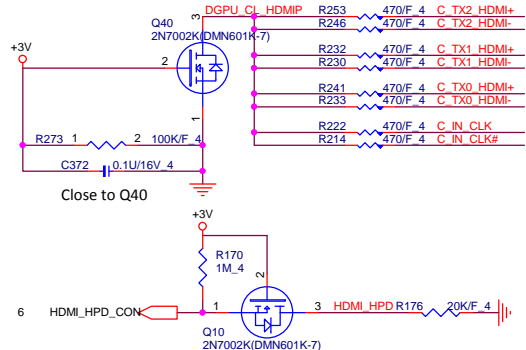
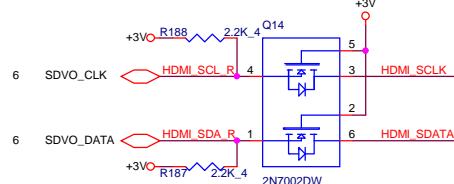
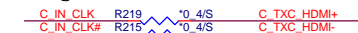




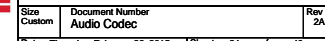
LID Switch

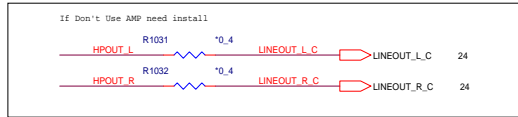


Change 220 ohm for EA 11/13 SI



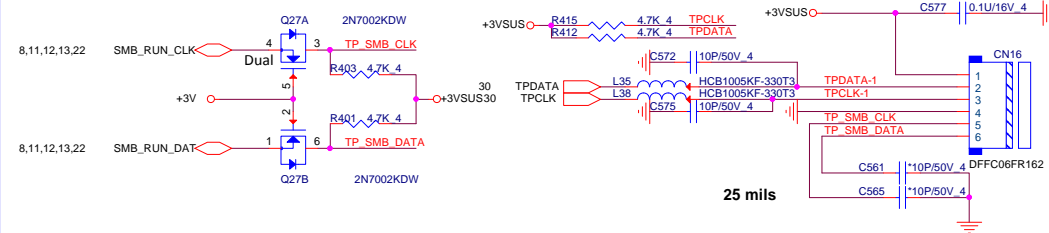
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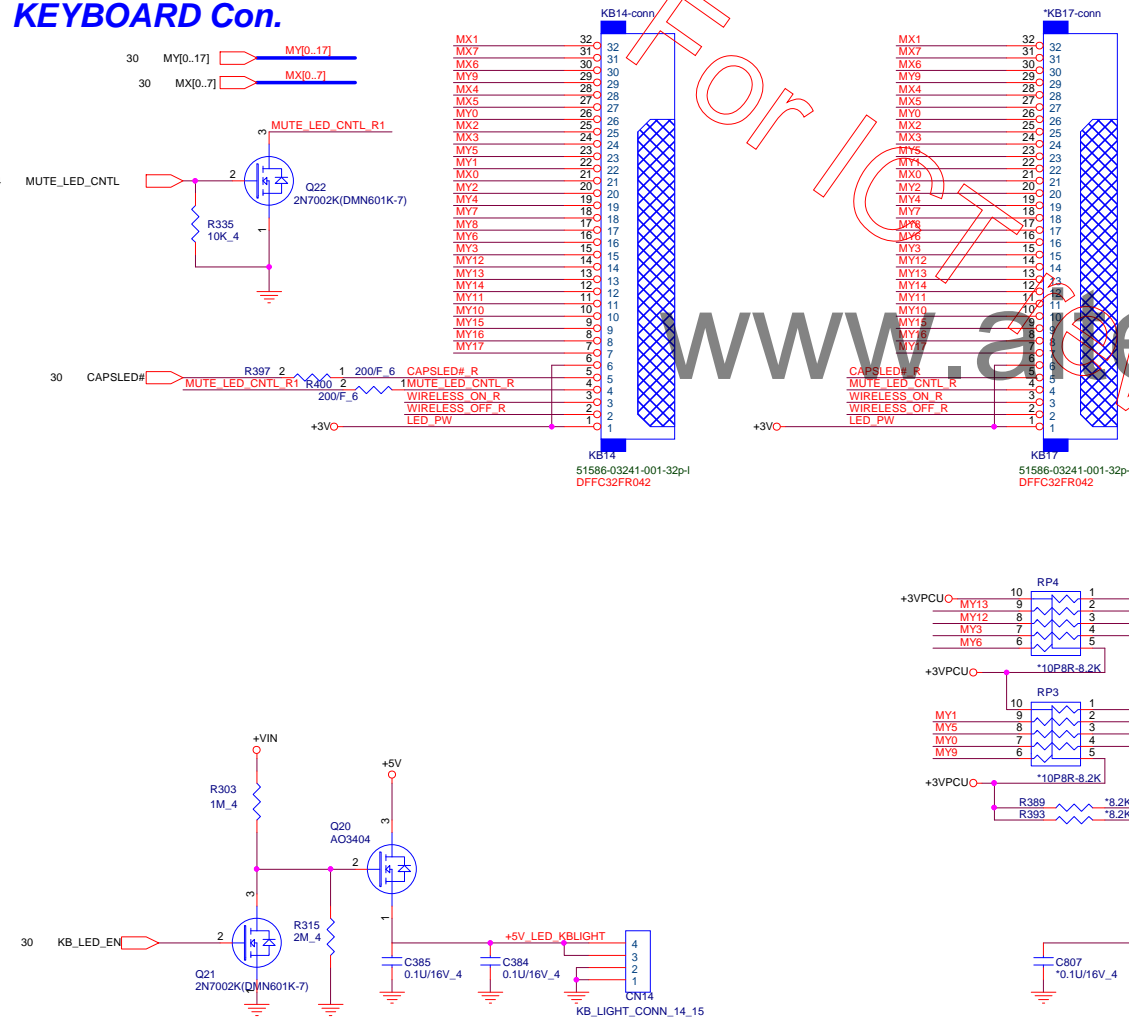


Pin	Function	I/O
1	L48	
2	PCIE_CLKREQ_CRP#	
3	PCIE_CLKREQ_CRP#	
4	USBP5+ C	
5	USBP5- C	
6	USB30_TX3+	
7	USB30_TX3-	
8	USB30_TX3+	
9	USB30_TX3-	
10	USB30_TX3+	
11	USB30_TX3-	
12	USB30_TX3+	
13	USB30_TX3-	
14	USB30_TX3+	
15	USB30_TX3-	
16	USB30_TX3+	
17	USB30_TX3-	
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22	USB30_TX3+	
23	USB30_TX3-	
24	USB30_TX3+	
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153	USB30_TX3-	

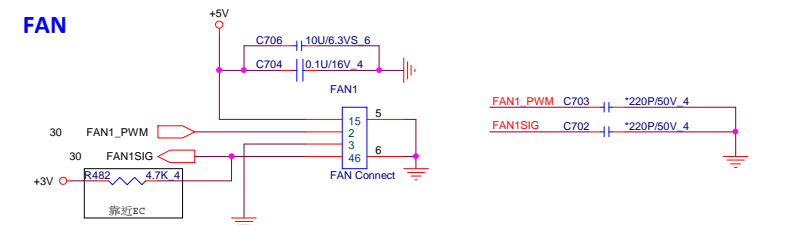
Touch Pad Connector



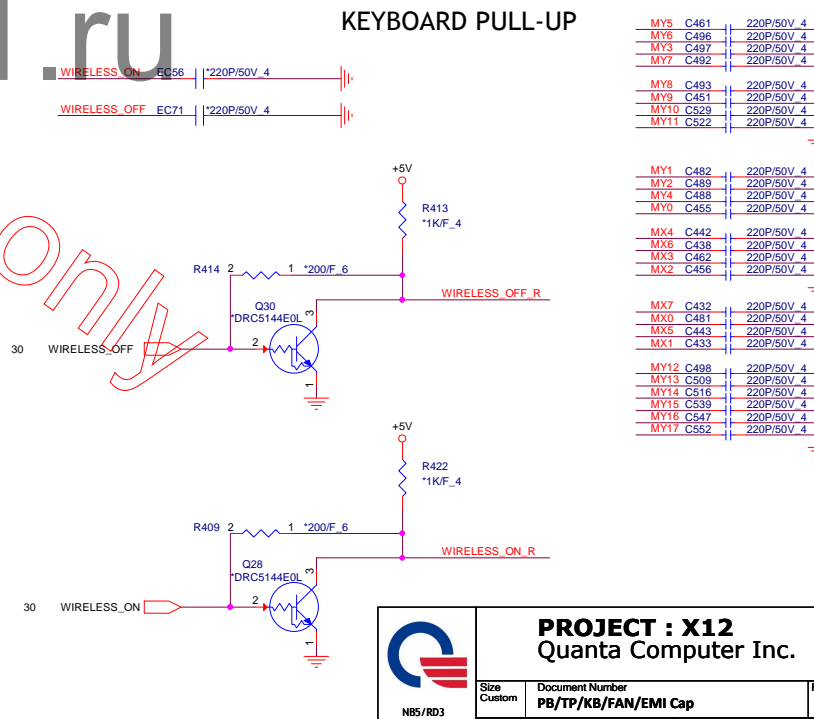
KEYBOARD Con.



FAN



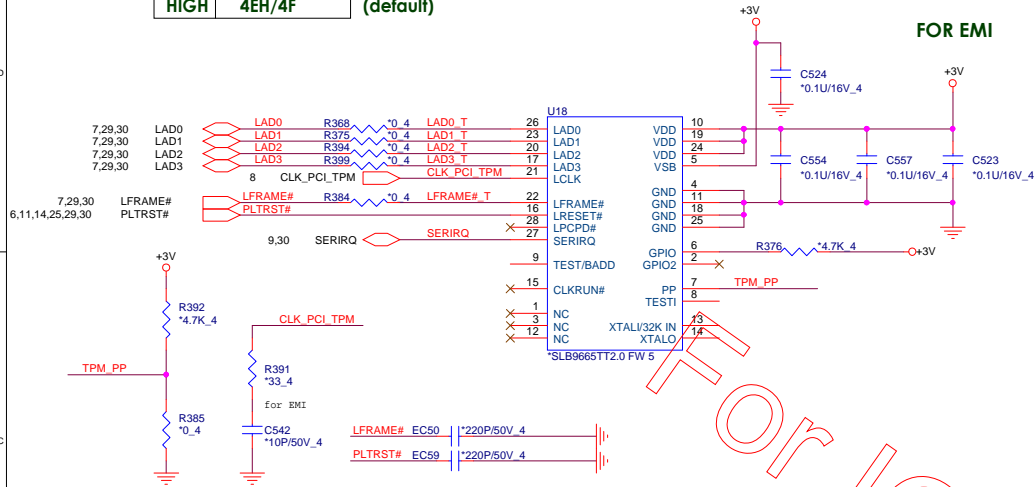
KEYBOARD PULL-UP



TPM (2.0)

Address

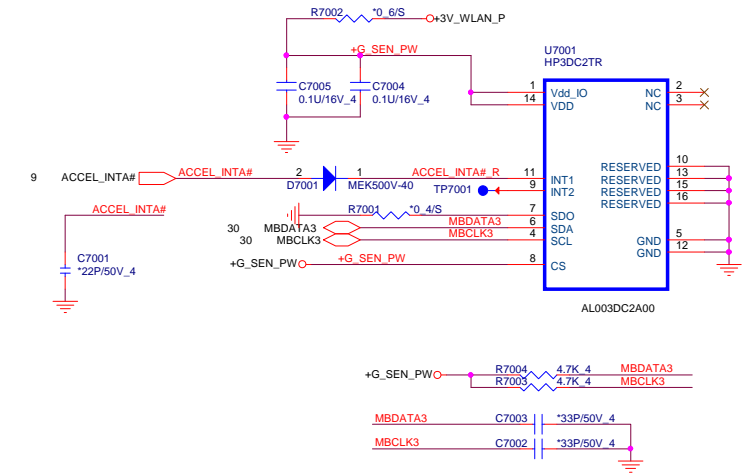
	BADD
HIGH	4EH/4F (default)



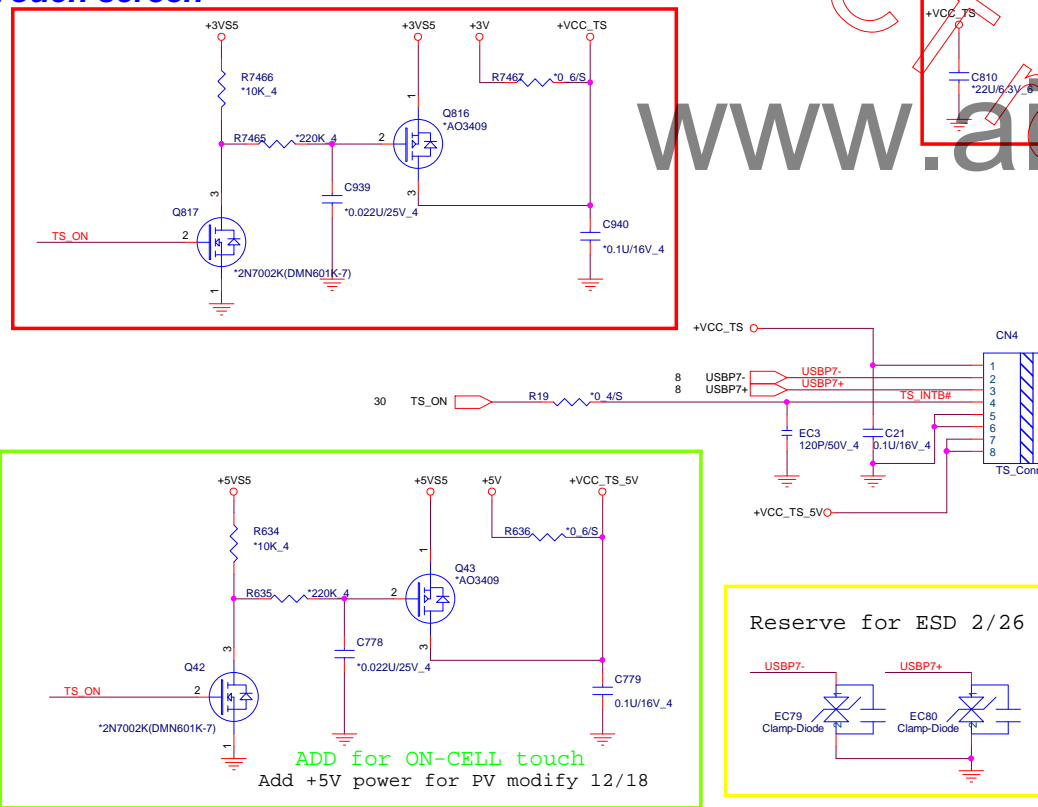
Accelerometer Sensor

27

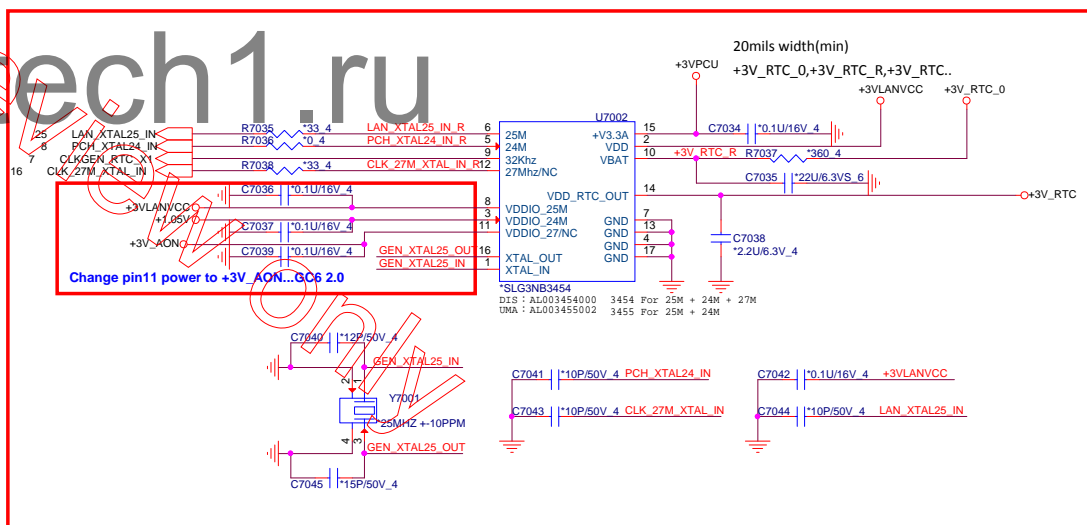
G-Sensor Power need check



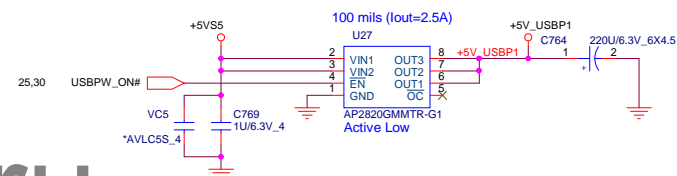
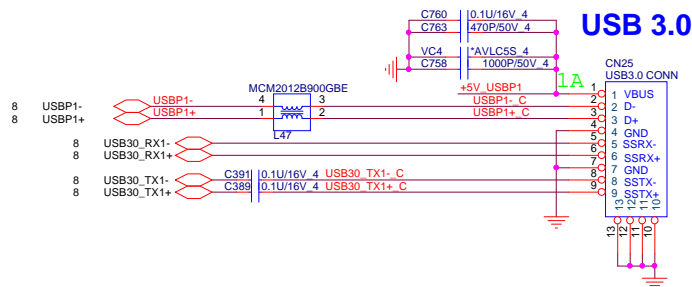
Touch screen



Green CLK Circuitry



Change Green CLK to Crystal 11/21 SI

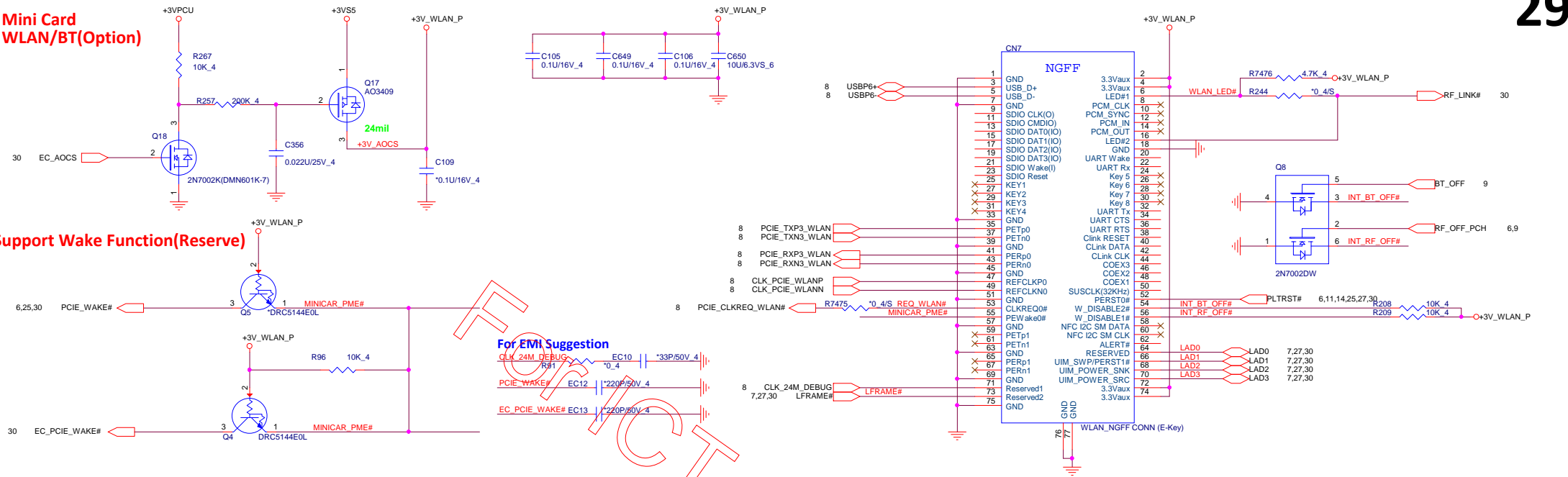


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EMI CAP

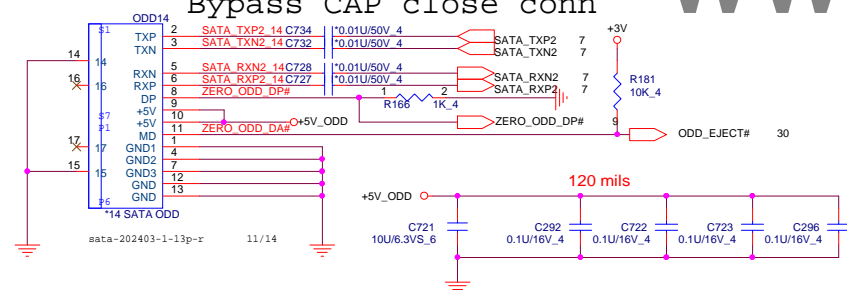
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+VIN	EC103	*0.1U/25V_4		+VIN	EC123	*0.1U/25V_4	
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+VIN	EC112	*0.1U/25V_4					
+VIN	EC113	*0.1U/25V_4					
+VIN	EC114	*0.1U/25V_4					
+VIN	EC115	*0.1U/25V_4					
+VIN	EC116	*0.1U/25V_4					
+VIN	EC117	*0.1U/25V_4					
+VIN	EC118	*0.1U/25V_4					
+VIN	EC119	*0.1U/25V_4					
+VIN	EC220	*0.1U/25V_4					

Support Wake Function(Reserve)

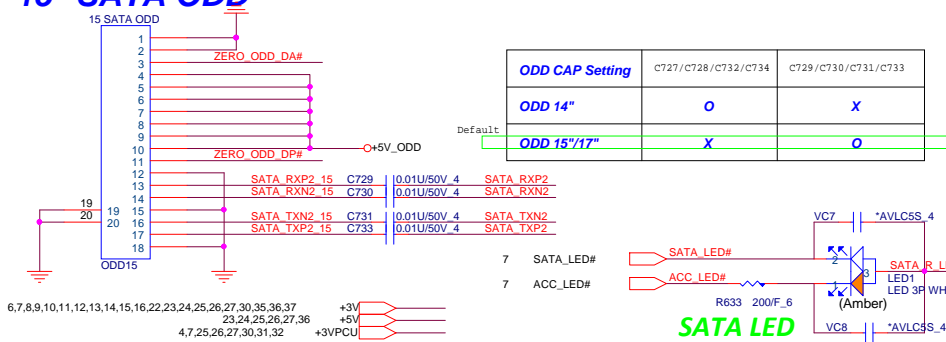


14" SATA ODD

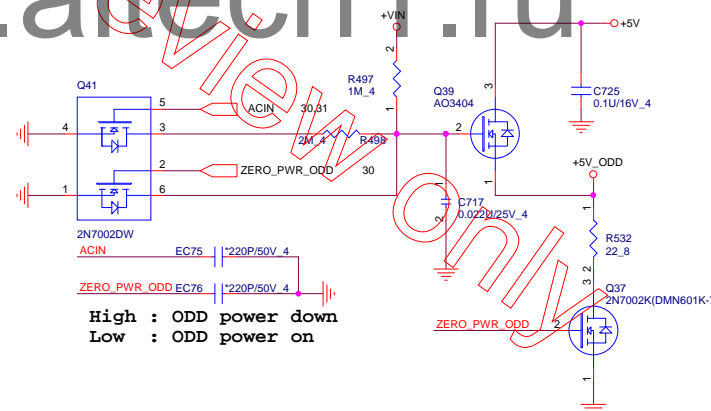
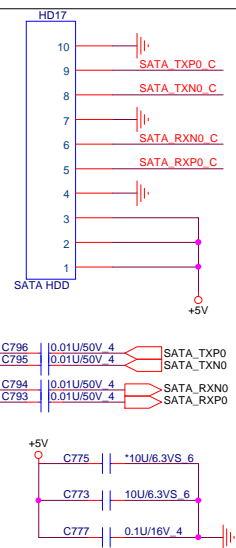
Bypass CAP close conn



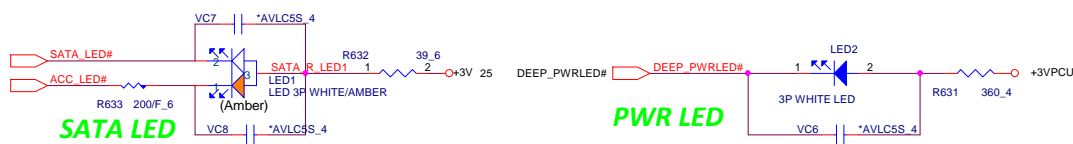
15" SATA ODD




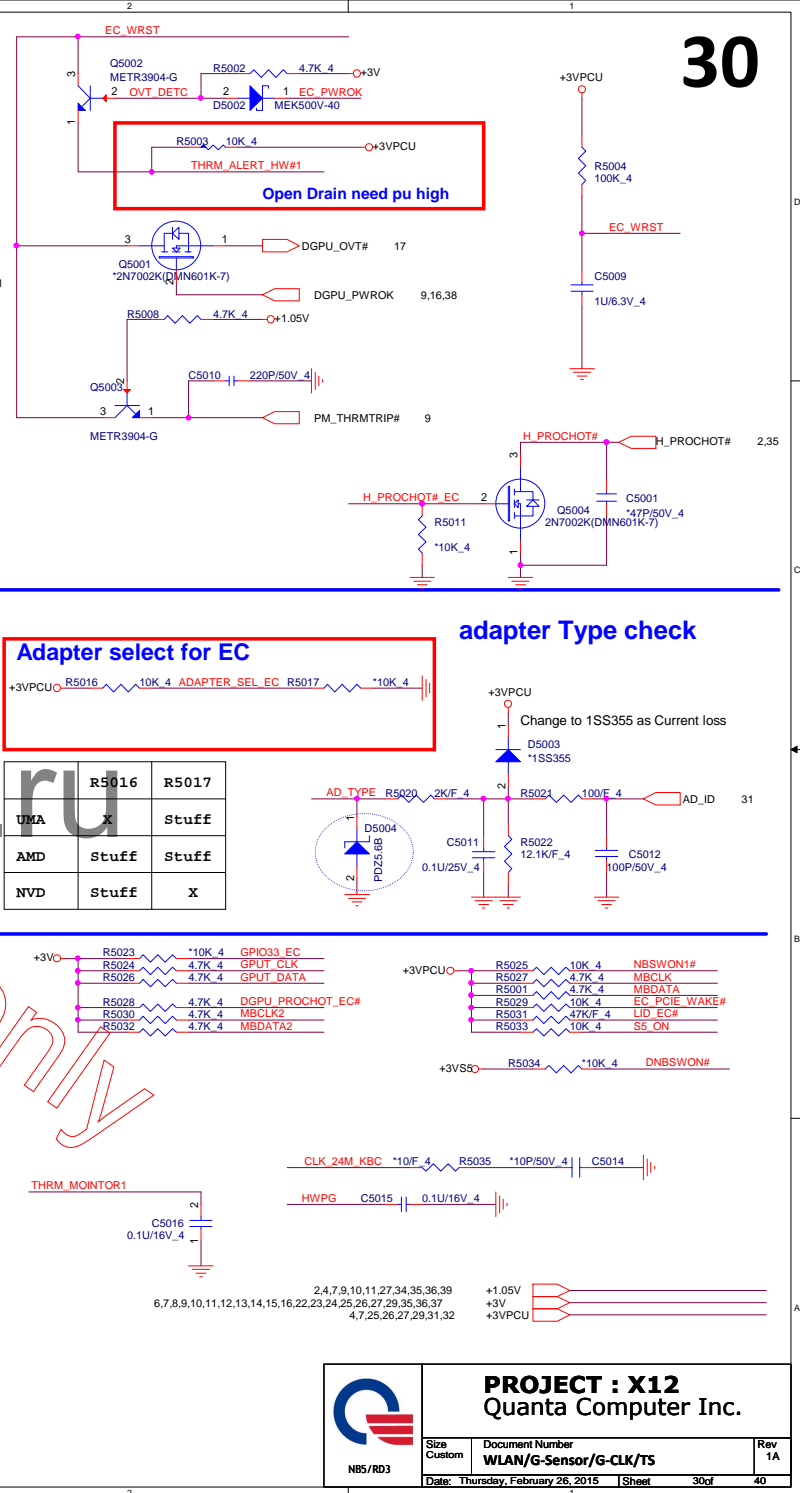
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HDD

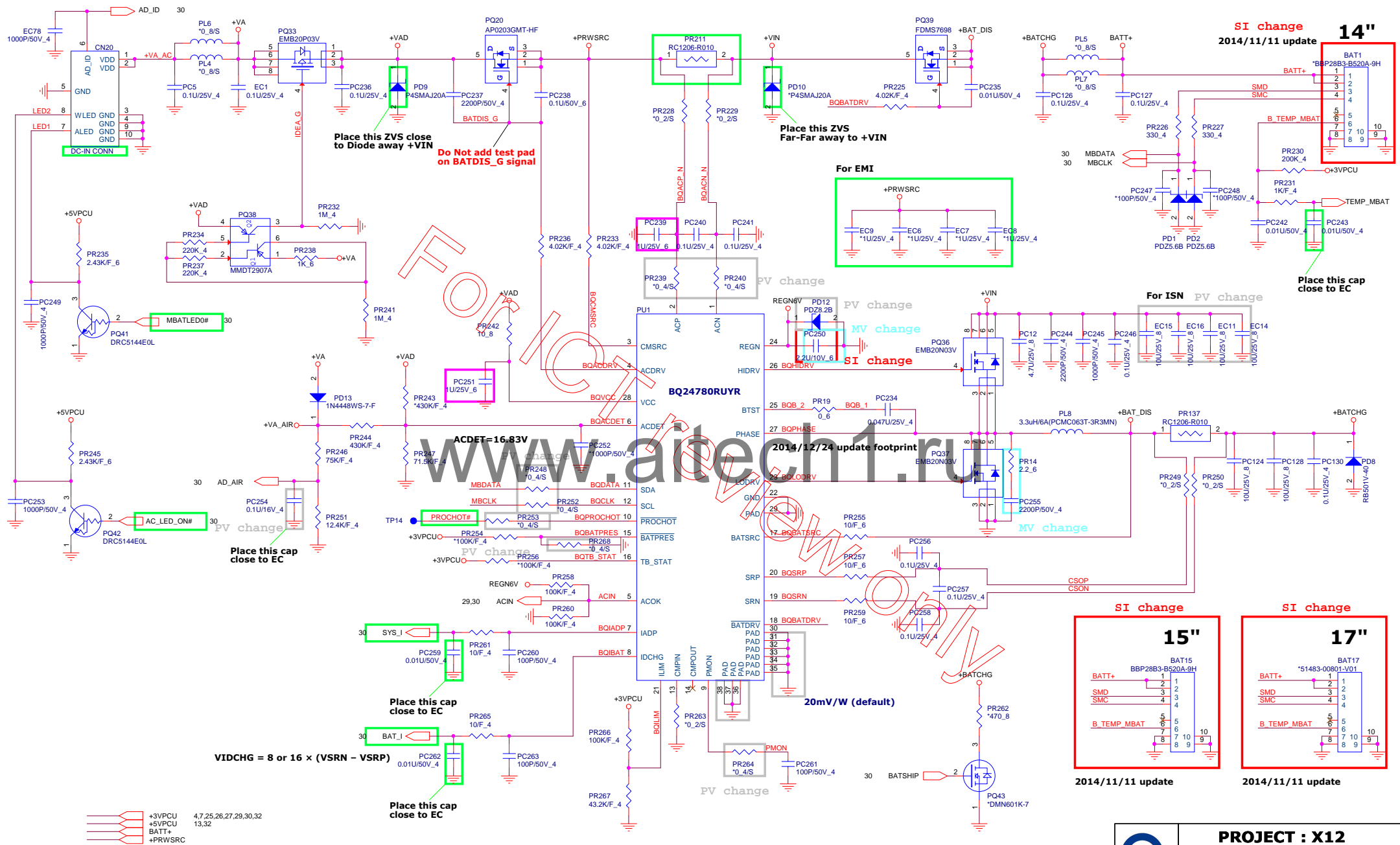
```
High  : ODD power down
Low   : ODD power on
```



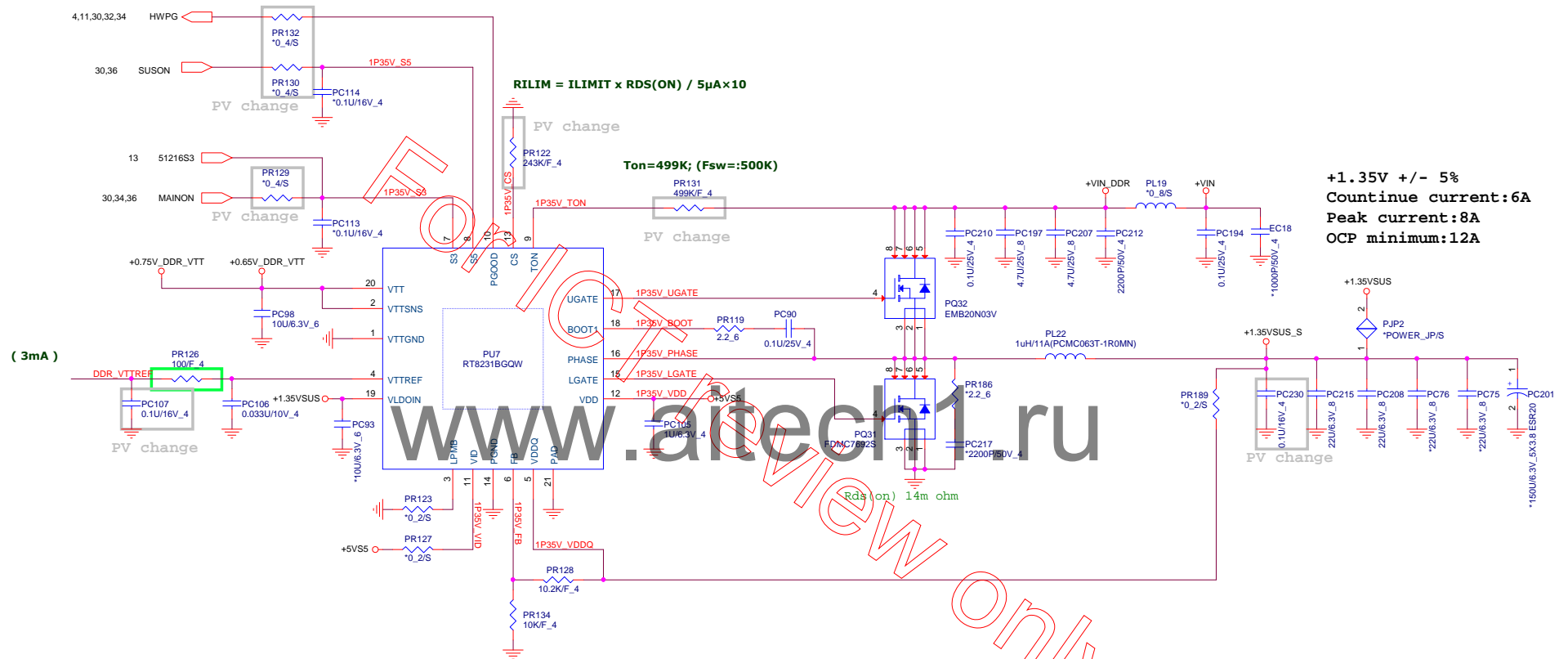
 NBS / RD3	PROJECT : X12 Qanta Computer Inc.		
	Size Custom	Document Number WLAN/NGFF/MSATA	Rev 1A
Date: Thursday, February 26, 2015		Sheet	29 of 40



90W DC JACK



USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff



+1.35V +/- 5%
Continue current:6A
Peak current:8A
OCP minimum:12A

+1.35VSUS

2 PJP2
POWER_ID:0

1

PC215 PC208 PC76 PC75 PC201

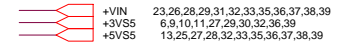
220u6 3V.8 220u6 3V.8 220u6 3V.8 220u6 3V.8 220u6 3V.8

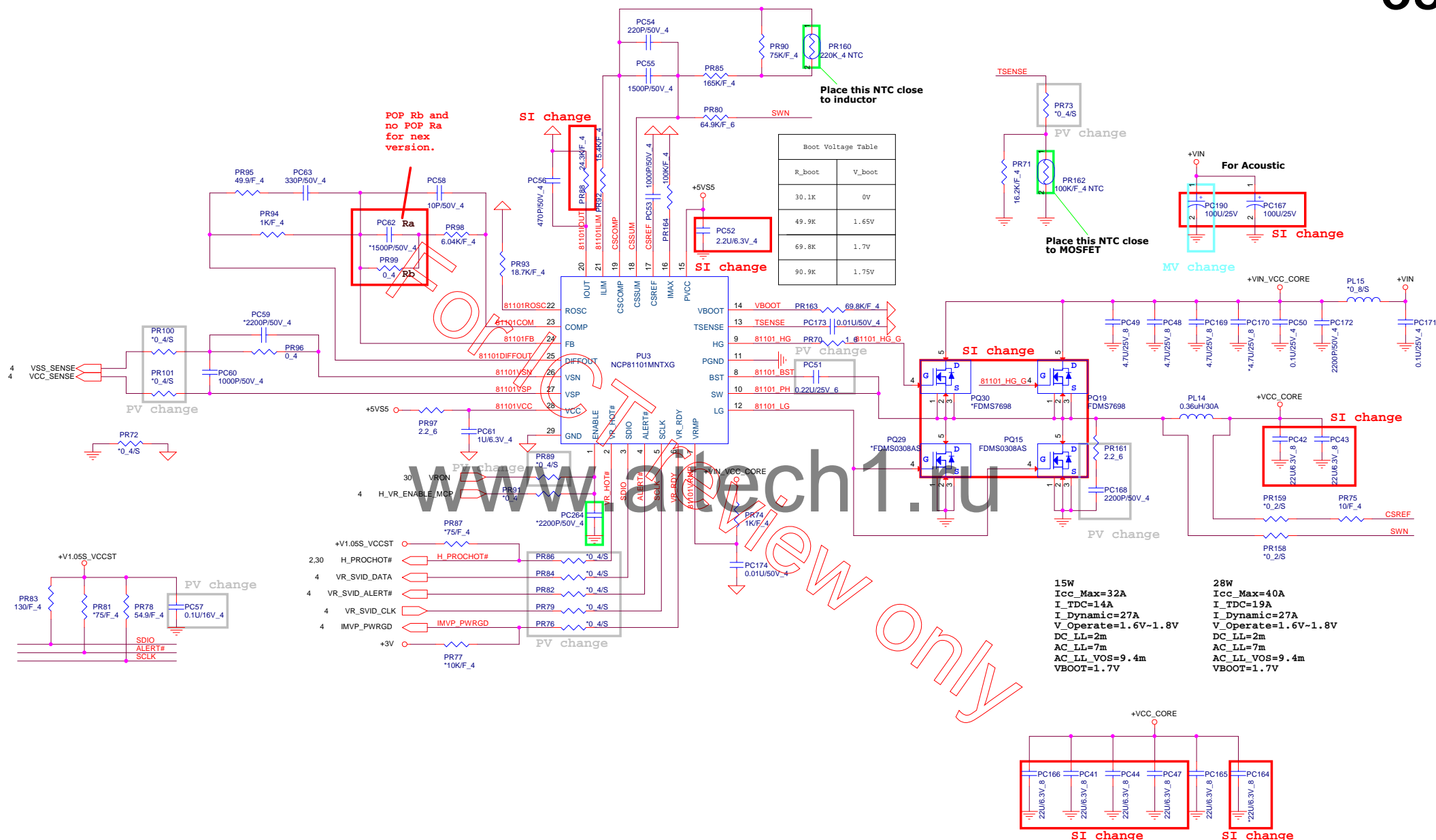
150U/6.3V_5X3.8 ESR20

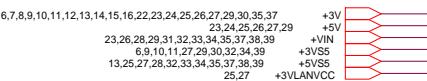
 +1.35VSUS 2,4,12,13

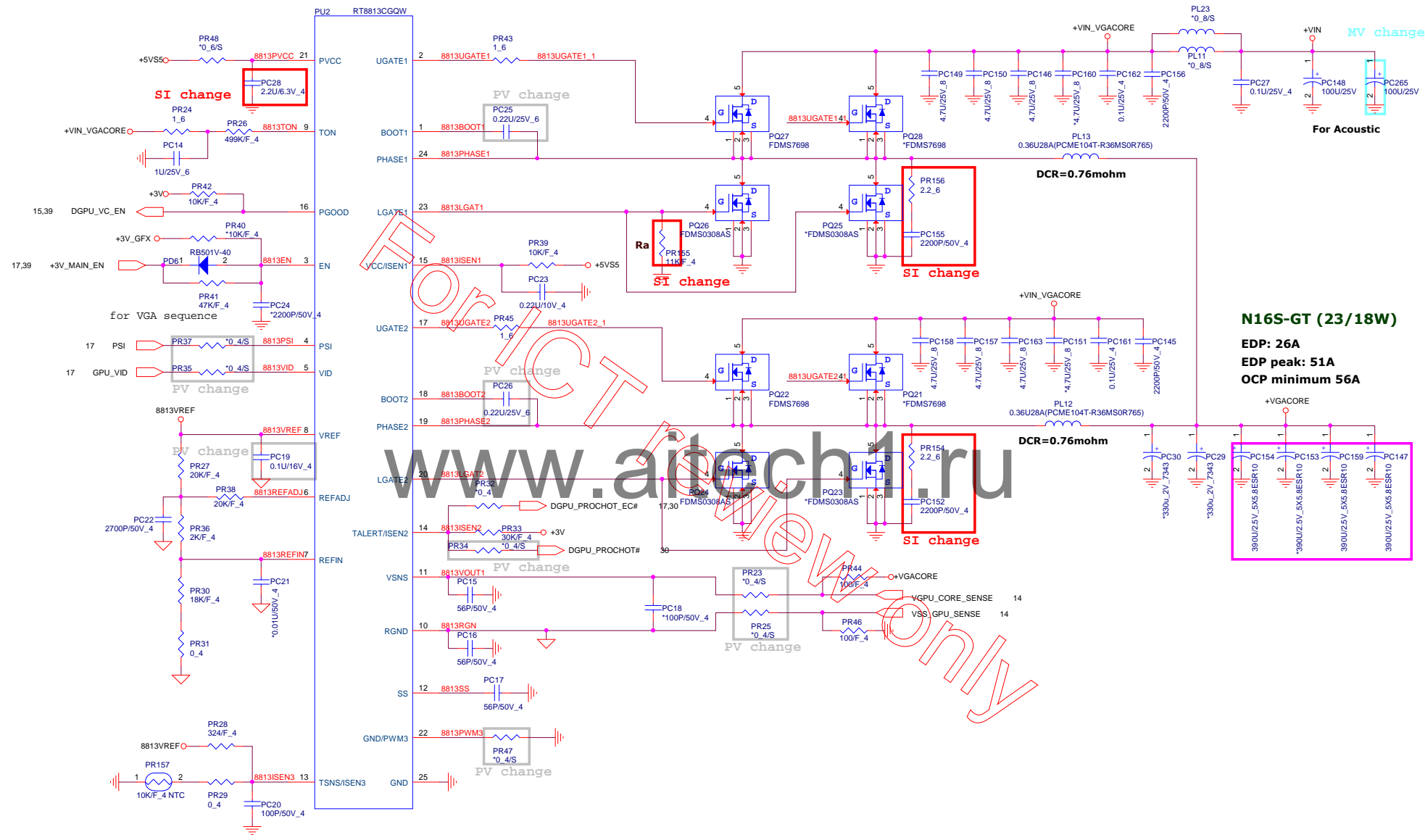
NB5/RD3

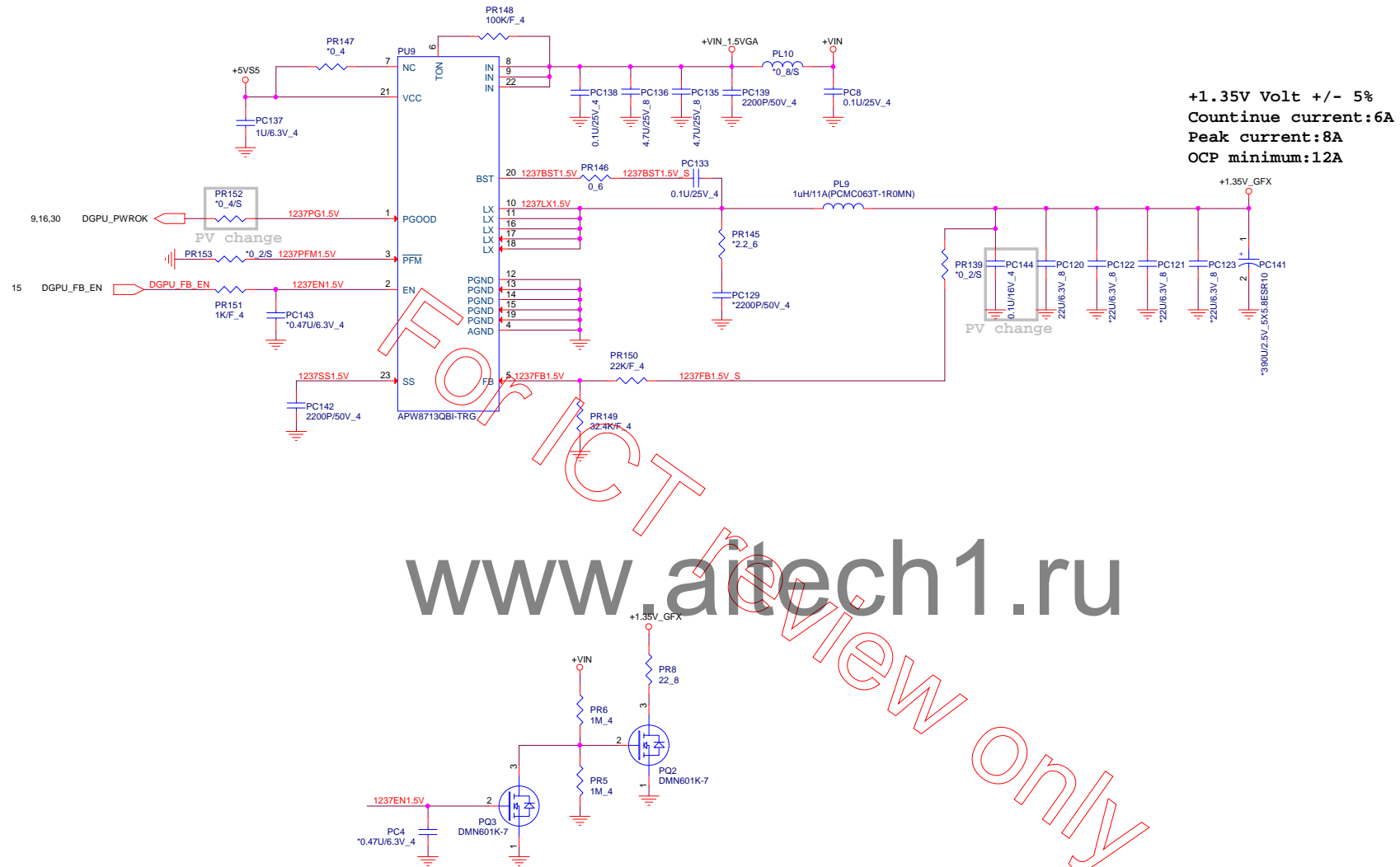
Size Custom	Document Number DDR3 (RT8231A)/1.8VS5	Rev 1A
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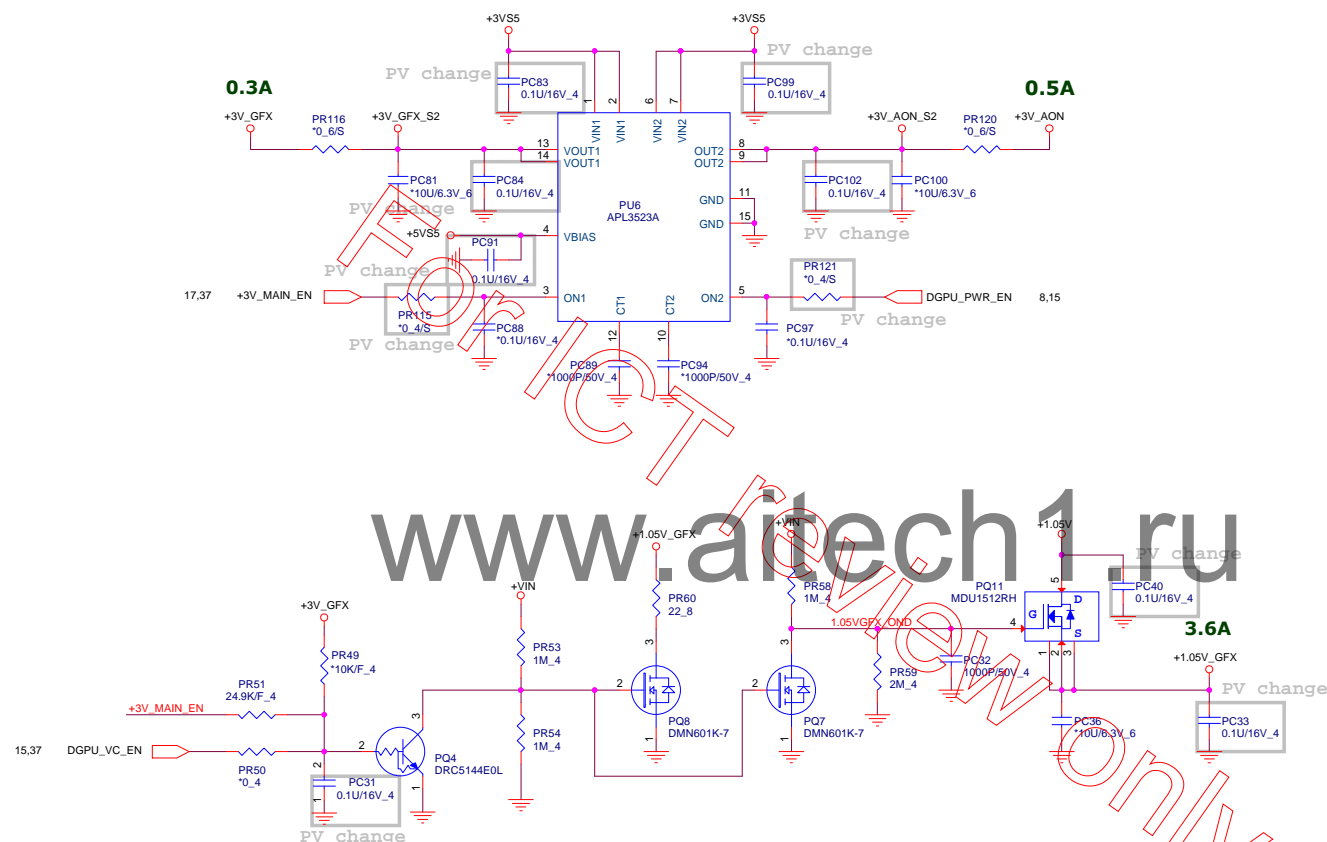










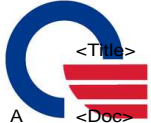


Battery Connector	Pavillion	ENVY
14"	-	-
15"	-	-
17"	-	-

USB Charge Support	PR185	PR184
Pavillion	Stuff	NA
ENVY (USB charge)	NA	Stuff

UMA	Disable Page 41、42、43 ,but keep below location
Page 41	PC161、PC162
Page 42	PC138、PC144、PC4、PC148
Page 43	PC84、PC102、PC88、PC97、PC40、PC33

Discrete	Location	Part Number
N15S (25W)	PR155	CS29532FB10
	PC151、PC160	NA
	PQ21、PQ23、PQ25、PQ28	NA
N15P (35W)	PR155	CS31242FB13
	PC151、PC160	Stuff
	PQ21、PQ23、PQ25、PQ28	Stuff

	PROJECT : X12		
	Quanta Computer Inc.		
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